Flying Probe Testing

PCBA Design for Testability

Design for Testability of Printed Circuit Board Assemblies

Test Engineer's Handbook

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Contents

Revisions

Version	Date	Comments
4	15.11.16	General review
5	15.12.16	Added chapters: • Via identification • Junction Scan • 2D Code Updated chapters • TH Pin • Panel of boards • Warped boards
6	06.10.17	Added chapter: • Multi Probe Unit (4080)
7	12.06.18	Modified chapter: • Multi Probe Unit (4080) Added chapter: • Measurement of light parameters • Side device interface (4080) • Programmable components

Introduction

The *Design for Testing* or *Design for Testability* (DFT) consists of a series of rules for the design of electronic boards in order to:

1. **Ensure the testability of each mounted component** *(In-Circuit Test)*;
2. **Simplify the testability of the functions** *(Functional Test)*;
3. **Allow for programming of the programmable components** *(On-Board Programming)*;
4. **Make the automatic test generation possible**
5. **Make the In-Line transport of the board possible**

The purpose of the production testing (*Manufacturing Test*) of an electronic board is to ensure that there are no defects, which may cause malfunction of the circuits or early on field failure of the mounted components. In addition, the purpose of Manufacturing Test is the production process control. This prevents the production line to start producing defects as the time goes by.

Each net of the circuit needs available Testpoints in order to allow the complete testing of each component and the automatic generation of the test program (ATPG).
This is to ensure the maximum failures coverage and the minimum cost of testing.

The flying probe tester can contact very small testpoints but it is recommended to use, where possible, the recommended size in order to increase the speed of contacting and to reduce the testing time.

In summary, this document contains:

1. the electrical design rules
2. the mechanical design rules
3. the design rules to increase of the testing performance

- **Legend**

Recommended requirement

Economic advantage to save on the cost of testing.

Advantage in terms of test program development time.

Reference in SPEA documentation for detailed information.

Caution

- **Abbreviations**

➢ FP	Flying Probe Tester
➢ UUT	Unit under test
➢ TPGM	Test program
➢ TH	Through hole
➢ SMD	Surface Mounted Device
➢ OBP	On Board Programming
➢ PCB	Printed Circuit Board
➢ PCBA	Printed Circuit Board Assembly
➢ QC	Quality Control

1. Testing with Flying Probe tester

1.1 Types of manufacturing processes for PCBA

The manufacturing process of the board to be tested will affect the choice of the design strategy of the board itself.
For this reason, it is essential to take the manufacturing process into account when adopting the Design For Testability rules.

Manufacturing processes:

1. Hi-Volume Manufacturing Test
2. Low-Med Volume Manufacturing Test
3. Prototype Test
4. Quality Control (QC) Process Test
5. SMD Line Set-Up Check
6. Repair Loop
7. Field Repair

1.2 Types of test for PCBA

The types of tests that will be executed on the board are also fundamental in the design strategy of the card.

Types of test:

1. In-Circuit Test Power Off
2. In-Circuit Test Power On
3. Short circuit test
4. Power supply test
5. Open pin test
6. Nodal impedance test
7. Nodal voltage test
8. Insulation test
9. On-Board Programming
10. Build-In-Self-Test
11. Boundary Scan
12. Functional test
13. Optical test
14. Laser test
15. Light test
16. Nodal waveform test

2. Electrical design rules

2.1 Contact points

The **contact point** is a contactable surface where it is possible to place a **Testpoint**.
A contact point can be made on any contactable surface (VIA, SMD Pad, Pad TH, Test Pad, etc.) with the following features:

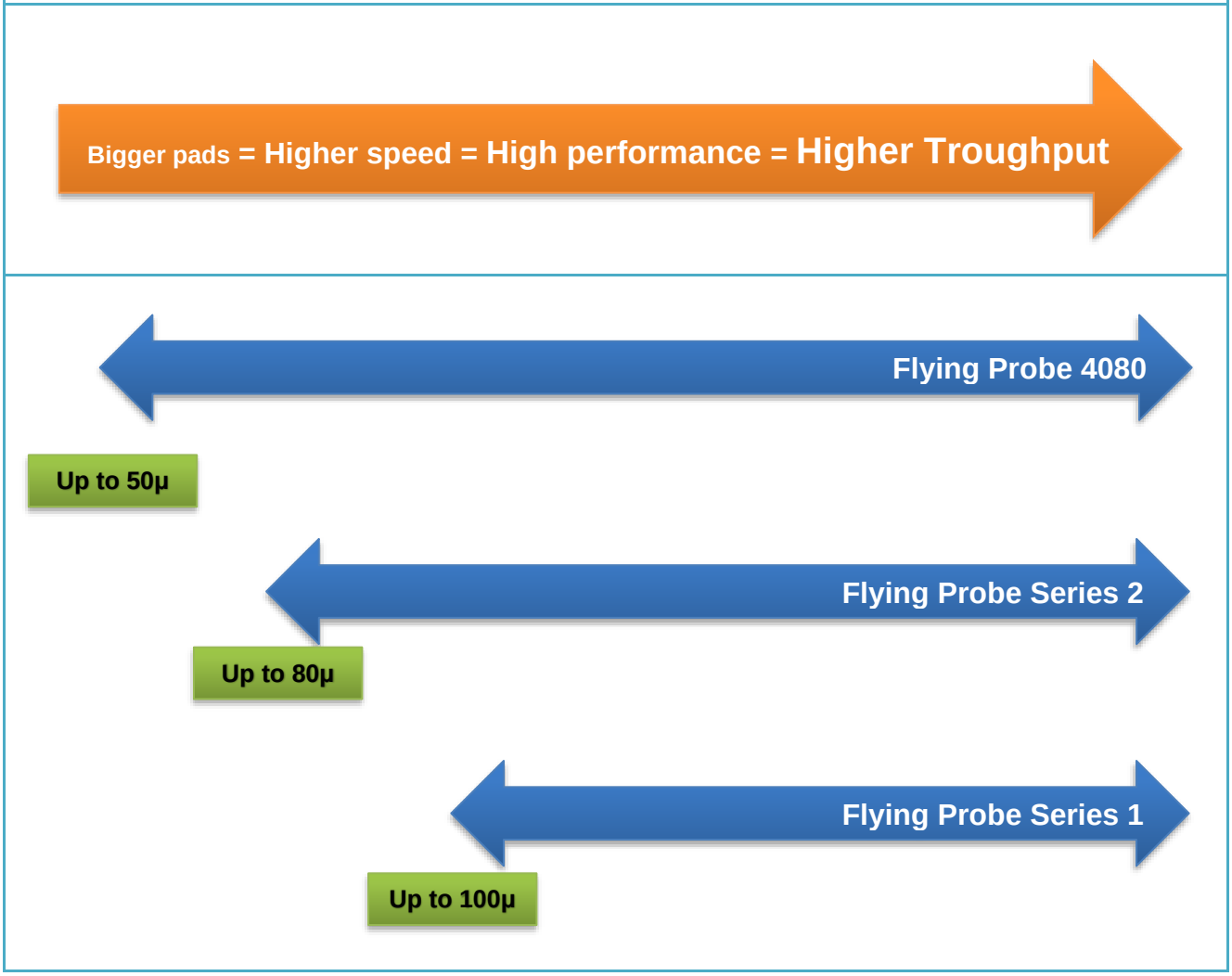
1. Flatness
2. Conductivity
3. Minimum dimensions
4. Accessibility
5. Located on the same level of PCB (recommended)

The testpoints are useful to contact the nets of the board under test in order to test:

1. The connected components
2. The absence of defects (short circuits, broken tracks, impedances)
3. The expected features

2.1.1 Minimum test point dimensions VS System capability

Minimum Dimension	...	...	...	...	...	Recommended Dimension
50x50 µm	80x80 µm	100x100 µm	200x200 µm	300x300 µm	400x400 µm	500x500 µm



Picture 1 – Relationship between size of the contact, test performance and system capability

2.1.2 Rules for the placement of test points

No.	Net Type	Minimum Test points net	Recommended Test point per net
1	**Analog**	1	>1
2	**Digital**	1	>1
3	**Not Connected**	1	1
4	**Power**	2	>2
5	**Ground**	2	>10
6	**Power supply**	2	>10

Table 1 – Quantity of test points per type of net

2.1.3 Distance of contact points from high components

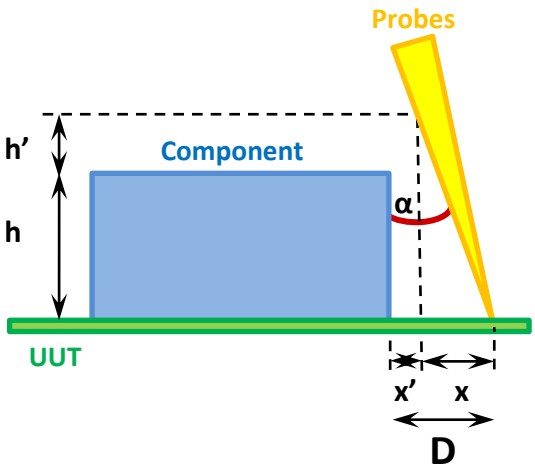
Components higher than 7mm, generate shaded areas that can affect the complete accessibility of the contact points in their surroundings. All the probes of the Flying Probe are affected by this concept.

This chapter suggests the rule to be used to obtain the maximum accessibility of the contact points by all the Flying Probe probes.

Applicability is valid for components up to 28mm in height.

In the case of components with a height between 28mm and 55mm, is required a specific study that takes care of the following aspects:

- Flying prove model (4 probes, 6 probes, 8 probes, manual, in-line, …);
- Open Pin Electro Scan present on axis;
- Light Meter (Led Color Sensor) present on axis.



Picture 2 – Maximum accessibility calculation

Symbol	Description
h	Component nominal height (max 28mm).
h'	3mm margin (to be considered for h> 5.5mm).
α	16° (is considered the axis with greater angle on 40xx S2). 13° (is considered the axis with greater angle on 4080).
x	Distance "margin - center of contact point" due to the projection of the nail.
x'	Margin of 2.5mm.
D	Clearance distance from "test point or contact point" (to be positioned beyond the D dimension).

Table 2 – Parameters

2.1.4 Priority of the contact points

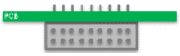
Priority	Type	Description	Drawing
1	**Test Pad**	Point of contact on the PCB arranged exclusively for testing and non-functional to the board.	
2	**Pad**	Point of contact on the PCB arranged as electrical requirement of the board (e.g. not mounted component, track terminations...).	
3	**Via**	Through hole connecting different layers of the PCB.	
4	**Pin TH**	Contact point created on the welding of a through hole component pin (mounted on one side and contactable on the other side).	
5	**Soldering Pad**	Contact point of the printed circuit with welded SMD components or of integrated circuit pins welded on it.	

Table 3 – Priority of the contact points

2.1.5 Test Pad

The Test Pads are the preferred contact points of the printed circuit, designed exclusively for testing and non-functional to the board.

The Test Pads allow contacting each net of the PCB, preventing the need to contact less than optimal contact points. It is therefore recommended to have at least a one test pad per net.

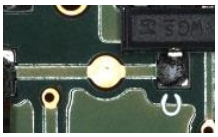
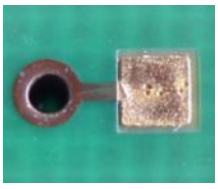
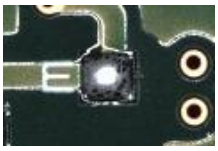
No.	Type	Layout	Example	Minimum dimension	Recommended dimension	Contacting capability
1	**Round**			Ø 70 µm	Ø 500 µm	**QUALIFIED**
				Ø 70 µm	Ø 500 µm	**QUALIFIED**
2	**Square**		 	70 x 70 µm	500 x 500 µm	**QUALIFIED** ☆
				70 x 70 µm	500 x 500 µm	**QUALIFIED**
3	**Embedded in a trace**		-	70 x 70 µm	500 x 500 µm	**QUALIFIED**
4	**Half round**		-	70 x 70 µm	500 x 500 µm	**QUALIFIED**
5	**Triangle**		-	70 x 70 µm	500 x 500 µm	**QUALIFIED**

Table 4 – Test Pad

2.1.6 Pad

Point of contact on the PCB arranged as electrical requirement of the board, but that can also be contacted for testing purposes.

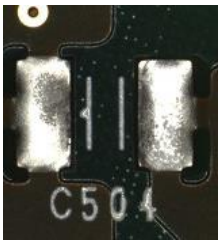
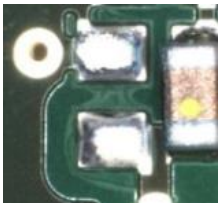
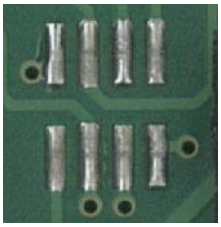
No.	Type	Layout	Example	Minimum dimension	Recommended dimension	Contacting capability
1	**SMD components**		  	70 x 70 µm	500 x 500 µm	**QUALIFIED**

Table 5 – Pad

2.1.7 Soldering Pad

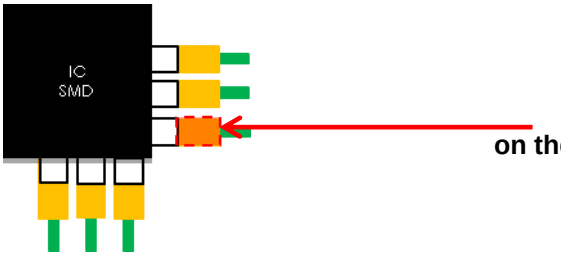
The soldering pad is the whole surface of the pad where the SMD component pin will be welded.

The area remaining after welding the SMD component pin can be used as a contact point:

Not mounted component

Mounted component

Contact point
on the pad of the mounted component



Contact point
on the pad of the mounted IC

Contact point on the pad
of the mounted component
with a placement error

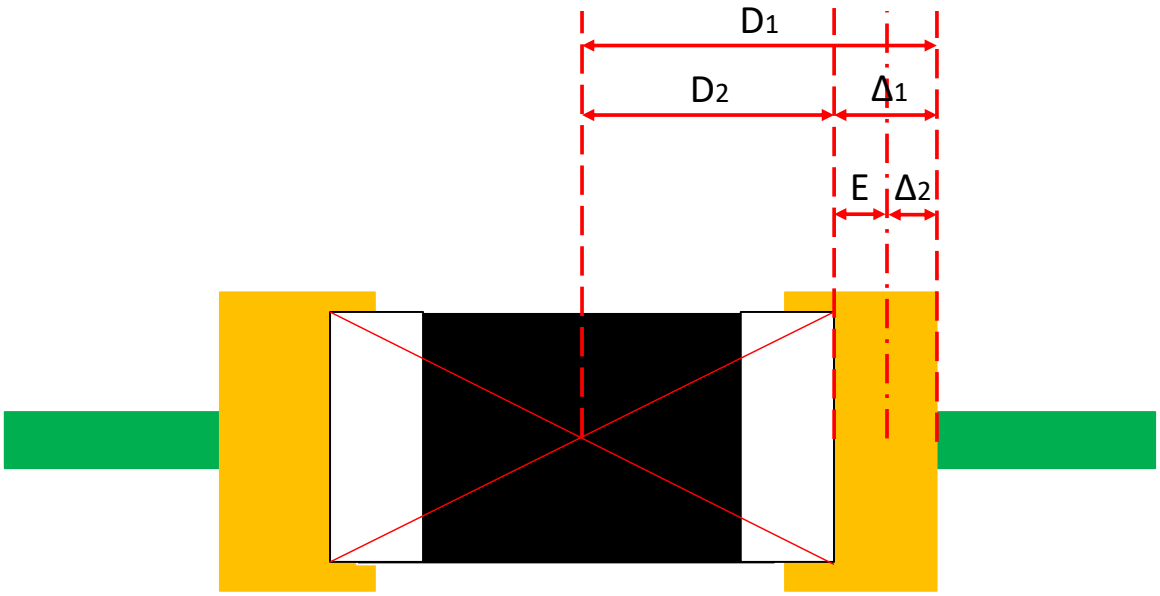
The positioning tolerance of the pick and place machine must be taken into account during the design of the pads of the PCB in order to create the contact point.
See next chapter

2.1.7.1 Component placement error

The placement error is the positioning tolerance of the pick and place machine when mounting the component.

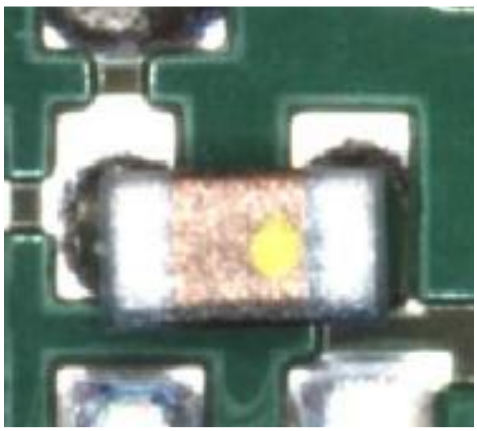
Consider the following during the board design process:

- This tolerance reduces the size of the contact point according to the formula in figure.
- The designer must consider this tolerance during the board design.
- The mounting tolerance is shown in the datasheet of the machine used for the manufacturing of the board.



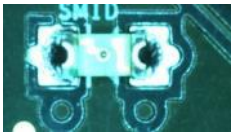
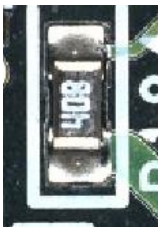
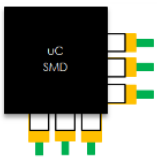
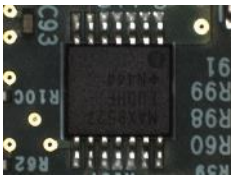
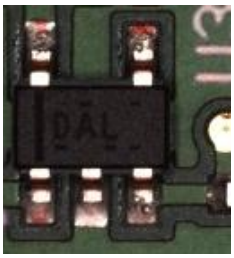
$\Delta_1 = D_1 - D_2$ Size of the pad without placement error

$\Delta_2 = D_1 - D_2 - E$ Size of the pad with placement error



Picture 3 – Example of placement error reducing the contact point

2.1.7.2 Types of soldering pads

No.	Type	Layout	Example	Minimum dimension	Recommended dimension	Contacting capability
1	**SMD Device pin**			70 x 70 µm	500 x 500 µm	**QUALIFIED**
				70 x 70 µm	500 x 500 µm	**QUALIFIED**
				70 x 70 µm	500 x 500 µm	**QUALIFIED** ☆
2	**SMD IC pin**			70 x 70 µm	500 x 500 µm	**QUALIFIED**
				70 x 70 µm	500 x 500 µm	**QUALIFIED**
				70 x 70 µm	500 x 500 µm	**QUALIFIED** ☆
				70 x 70 µm	500 x 500 µm	**QUALIFIED**

* The minimum pad must include the possible placement error. See dedicated chapter.

Table 6 – Soldering pads

2.1.8 Via

Vias are through holes that connect the different layers of the PCB.

A contactable via must not be covered with insulating material and adhere to the mechanical properties below.

2.1.8.1 Via geometry

The geometry of the via should be designed in function of the number contactable and available vias for each net of the board.
The following table shows the contact area to design on vias to make them contactable:

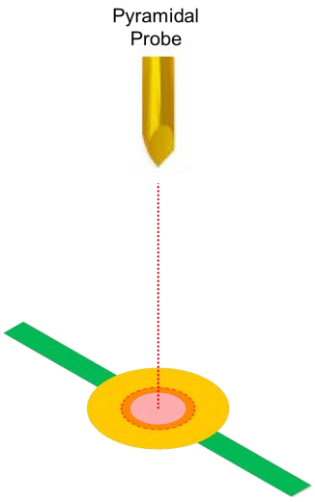
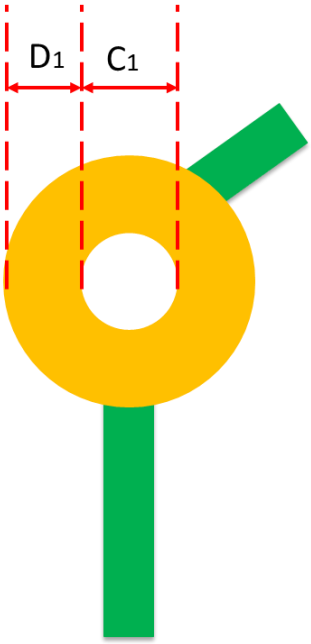
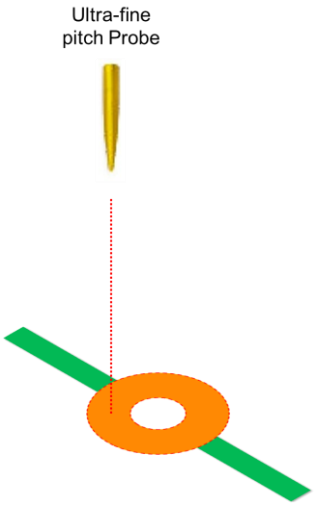
No.	Full Board accessibility using vias only	Contact area on via	Geometry	Dimensions
1	YES			C1 = 100÷400 µm D1 > 100µm
2	NO			D1 > 150µm

Table 7 – Contacting areas on via

2.1.8.2 Types of Vias

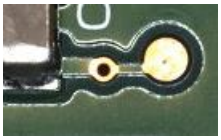
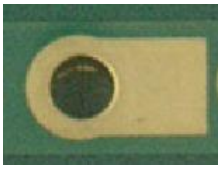
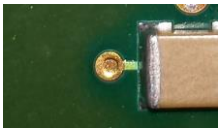
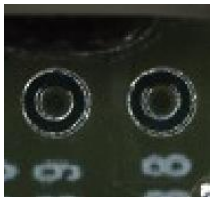
No.	Type	Layout	Example	Contacting Capability
1	**Round through hole**			**QUALIFIED**
2	**Square or rectangular through hole**		-	**QUALIFIED**
3	**Through hole followed by pad**			**QUALIFIED**
4	**Blind round**			**QUALIFIED**
5	**Blind square / rectangle**		-	**QUALIFIED** ☆
6	**Coated**			**NOT QUALIFIED**

Table 8 – Via

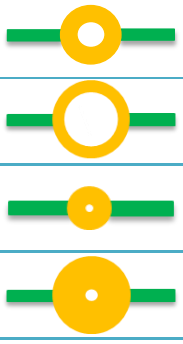
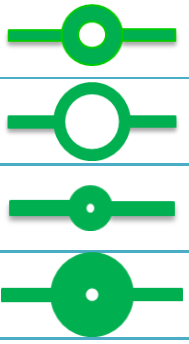
2.1.8.3 Via identification

The vias may differ in the following characteristics:

A. **Different Geometries**
B. **Covered by solder mask**
C. **Covered or not covered by components**
D. **Mounting on layer**

Depending on the characteristics of the vias on the board to be designed, the vias must be identified with a different part number for each case so they can be used in a simple and effective way during the development of the test program.

- **Cases**

Case A	Case B
Different Geometries	**Covered by solder mask**
	

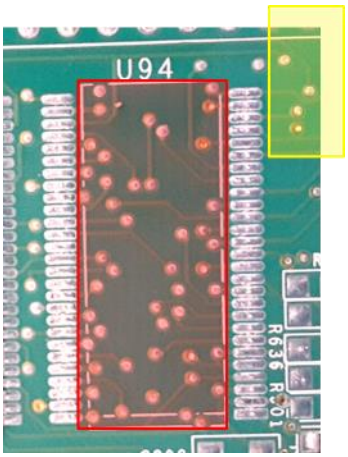
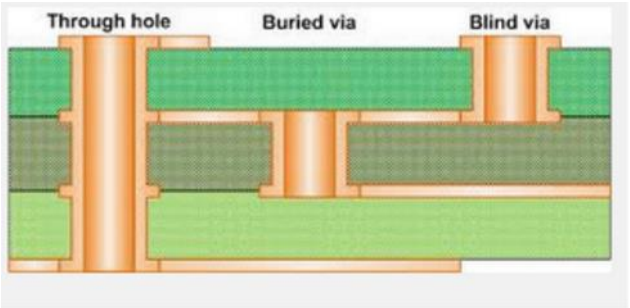
Case C	Case D
Covered or not covered by components	**Mounting on layer**
	

Table 9 – Identification of the vias through part number

2.1.9 TH Pin

A Through Hole (TH) Pin is a pin of vertical mounting axial components, mounted on one side of the board and accessible on the other.

The typical pitch of TH components is 2.54 mm.

The following table shows the contact area to design to allow touching on TH Pins:

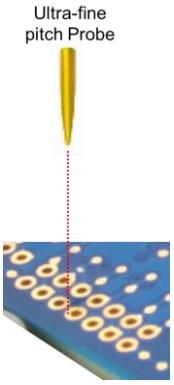
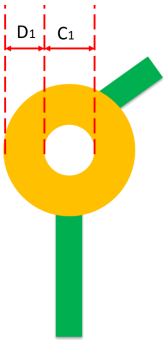
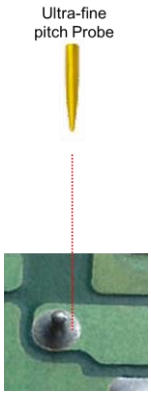
No.	Type	Example	Contact point on TH pin	Geometry	Contacting Capability
1	**Not mounted component**			 D1 > 150µm	**QUALIFIED**
2	**Mounted component**			-	**QUALIFIED**
			 Greasy welding	-	**NOT QUALIFIED**
3	**Not mounted component with tinned hole**			-	**QUALIFIED** ☆

Table 10 – Contact point on TH pin

2.2 Circuit configurations

An electronic board can encompass particular circuit functions which, when designed under ideal condition, can influence the coverage of the test program developed on FP.
The suggestions in the following chapters point to define an ideal route to making the board suitable not only for classic In-Circuit test, but also for functional test, devices programming, power-on tests etc.

2.2.1 Initialization circuits and electrical constraints

Some signals of the UUT may have to assume a certain state during a certain type of electrical testing.
This state can be decisive for their operation and may need to be configured generically before starting the test (In-Circuit, functional, programming, etc ...).

Examples of typical initialization circuits or electrical constraints:

1) Reset circuits
2) Constraints between grounds or power supplies
3) Active high constraints
4) Active low constraints

Provide for accessibility of the constraints through the following contact points:

1) Test Pad
2) Pad
3) Soldering Pad
4) Via
5) Connector

Avoid having a constrained signal useful for the test set only between two components with BGA technology.

In this case, such a signal can never be contacted to be tested.

2.2.2 Frequency measurements

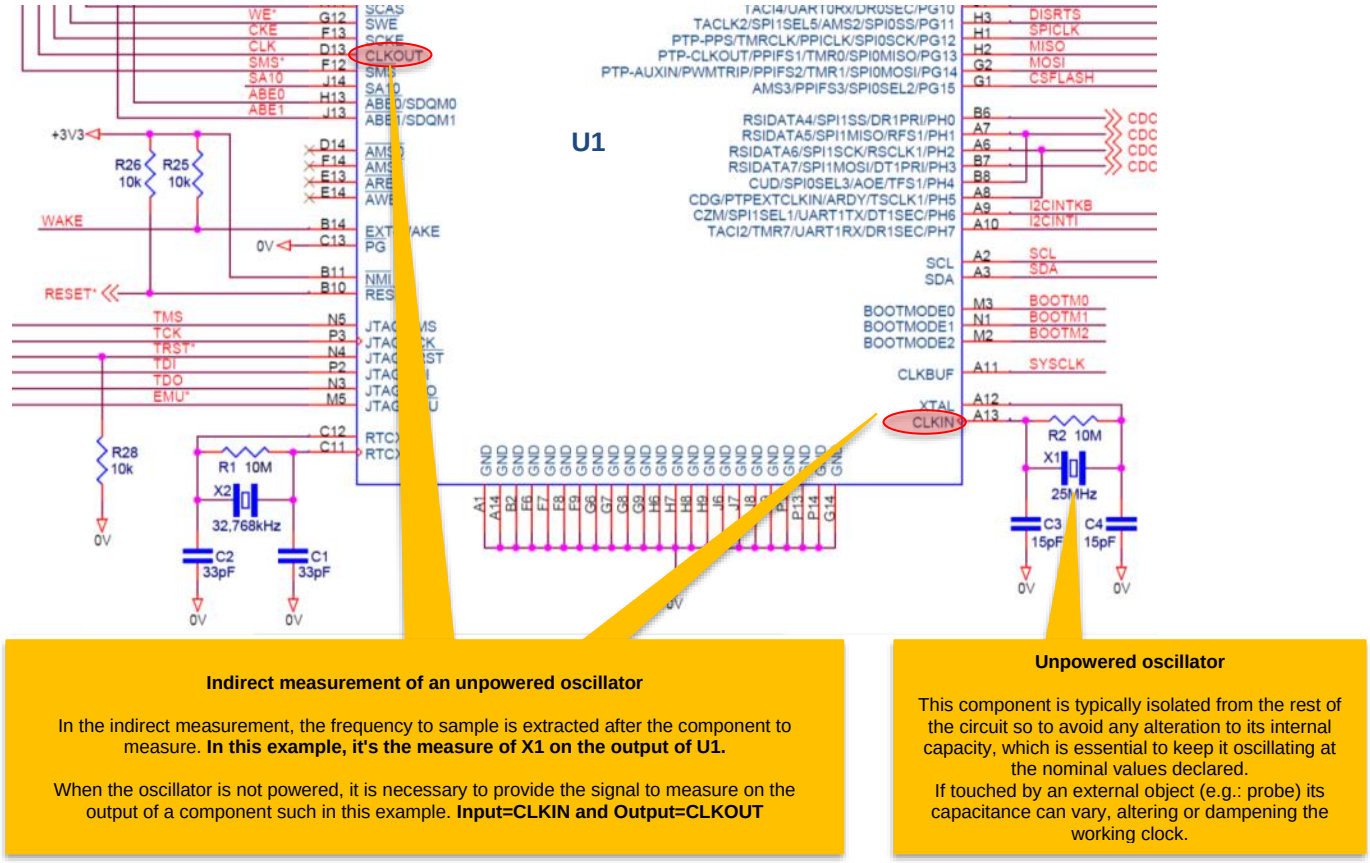
The FP is able to execute frequency measurements through the probes thanks to the electronics mounted on the axes themselves.

Two types of measurement exist:

1) **Direct measurement:** executed at the output of the component generating the frequency itself. It can be applied to measure signals not affected by the use of any measurement probe (e.g.: powered oscillators).

2) **Indirect measurement**: executed after the component generating the frequency, therefore on another component.
To measure a quartz, design the board so to have a downstream circuit where for the application of this measurement mode.

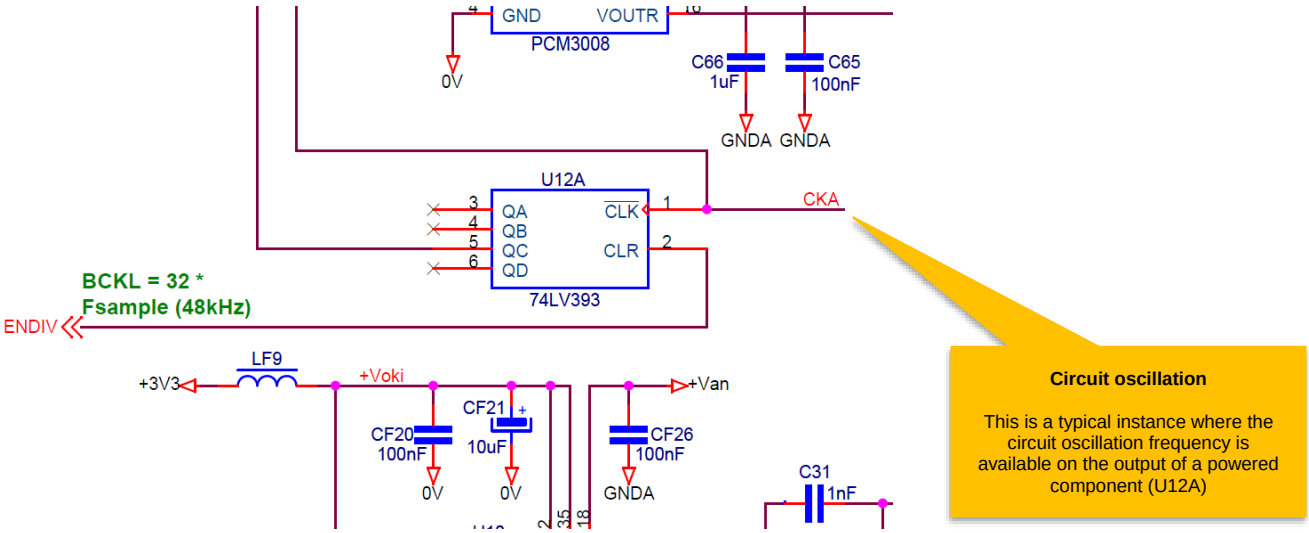
- **Example**



Picture 4 – Example of an indirect measurement of an unpowered oscillator.

Board Power On

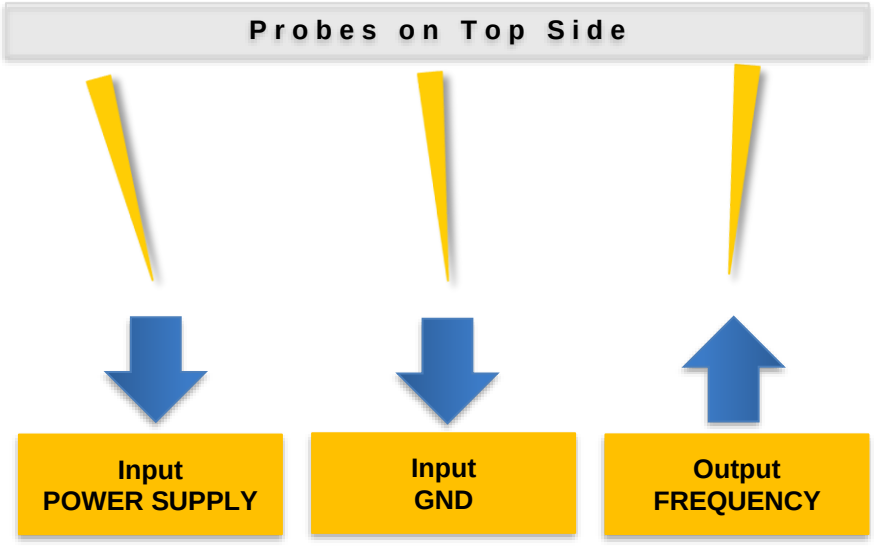
In this case it's better to power on the part of the circuit generating the signal under measurement.
If that's not possible, the whole board has to be powered in order to measure the U12A output frequency.



Picture 5 – Example an indirect measurement of the circuit oscillation

€ Arranging a pin on the output of a component to measure the clock of the board allows increasing the test coverage on FP, saving on the setup of an eventual functional test.

€ Designing all the necessary points to measure an oscillation (Power supply, GND and Output) on the same side of the board allows simplifying and speeding up the implementation of a test in an FP program.



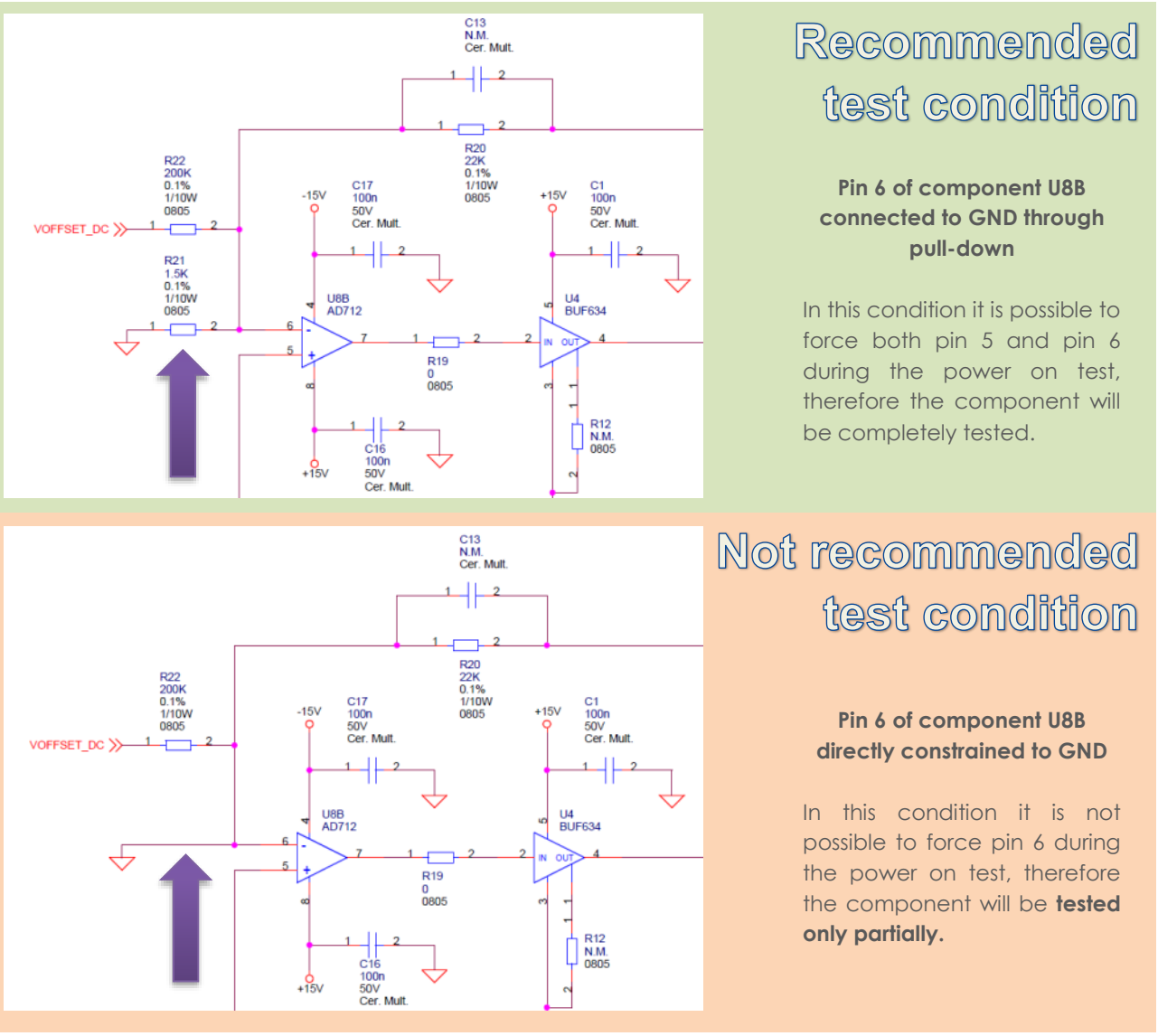
Picture 6 – Probes involved in a frequency measure

2.2.3 Designing for High and Low signal constraints

The FP test program can include Power On tests to verify the correct functioning of the analog and digital integrated circuits. On some of the pins of these components, the level of the signal can be constrained to high (e.g.: VCC) or low (e.g.: GND) due to electrical reasons. Fig. 2.1.3.a shows two methods to design Low signals constraints.

When aiming to increase the test coverage through the power on test, it's useful to arrange pull-up or pull-down resistors for the constrain of high and low signals, thus helping to enhance the test performance.

By designing pull-up and pull-down resistors to constrain signals to high or low, it's in fact possible to execute the power on tests by forcing all the inputs of the component to be tested (which would be impossible to do if the pin had been directly constrained through GND or VCC).



Picture 7 - Example of design of a signal constrained to GND.

Designing pull-up or pull-down resistors increases the tests applicable to the integrated circuit, consequently improving its test coverage.

3. Mechanical design rules

3.1 Fiducial

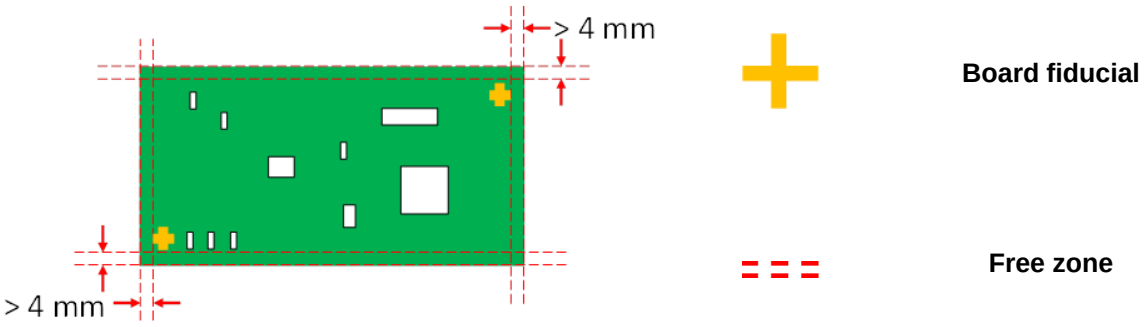
Board fiducials are elements designed to allow to recognize the UUT orientation inside the test area.

- **Characteristics**

No.	Characteristic	Requirement
1	Designed on CAD	RECOMMENDED
2	Not tin-plated	RECOMMENDED
3	Not covered by solder mask	RECOMMENDED
4	Surrounding area free of copper traces or screen-printed signs	MINIMUM
5	Surrounding area free of similar components	MINIMUM
6	(Asymmetrically) placed on the corners of the board	MINIMUM
7	Placed both on top and of bottom of the board	RECOMMENDED
8	Placed as externally as possible	MINIMUM
9	High-contrast color compared to PCB	MINIMUM

Table 11 – Fiducial characteristics

- **Position on the board**



Picture 8 – Fiducial position on the board

- **Suitable geometry**

No.	Shape	Minimum Dimension	Recommended Dimension	Catching Capability
1		500x500 µm	800x800 µm	QUALIFIED
2		500x500 µm	800x800 µm	QUALIFIED
3		500x500 µm	800x800 µm	QUALIFIED ☆
4		500x500 µm	800x800 µm	QUALIFIED
5		500x500 µm	800x800 µm	QUALIFIED
6		500x500 µm	800x800 µm	QUALIFIED

Table 12 – Suitable fiducial geometry

Designing the fiducials according to the criteria in this chapter increases its repeatability during board manufacturing and saves test time. This leads to greater overall throughput.

3.1.1 Alignment Fiducials on panel of boards

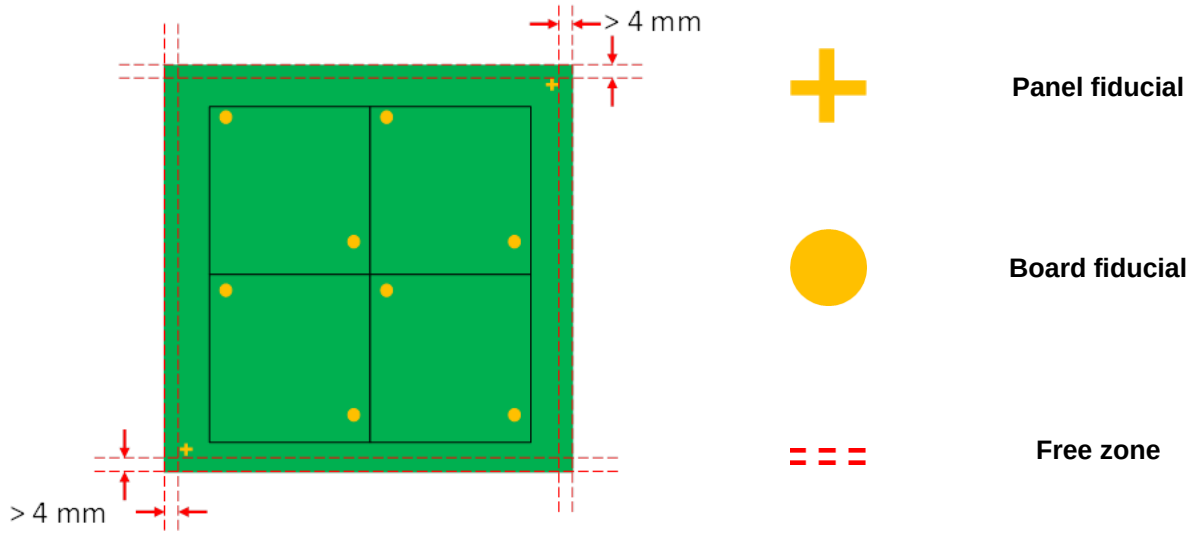
Panel fiducials are elements designed to recognize the orientation of the panel of boards.

The panel fiducials can be used when there is no specific need to use fiducials for the single board.
If used in place of the board fiducials, the alignment process will take less time, improving the performance of the test program.

- **Characteristics**

  Refer to the Fiducial chapter.

- **Position on panel**



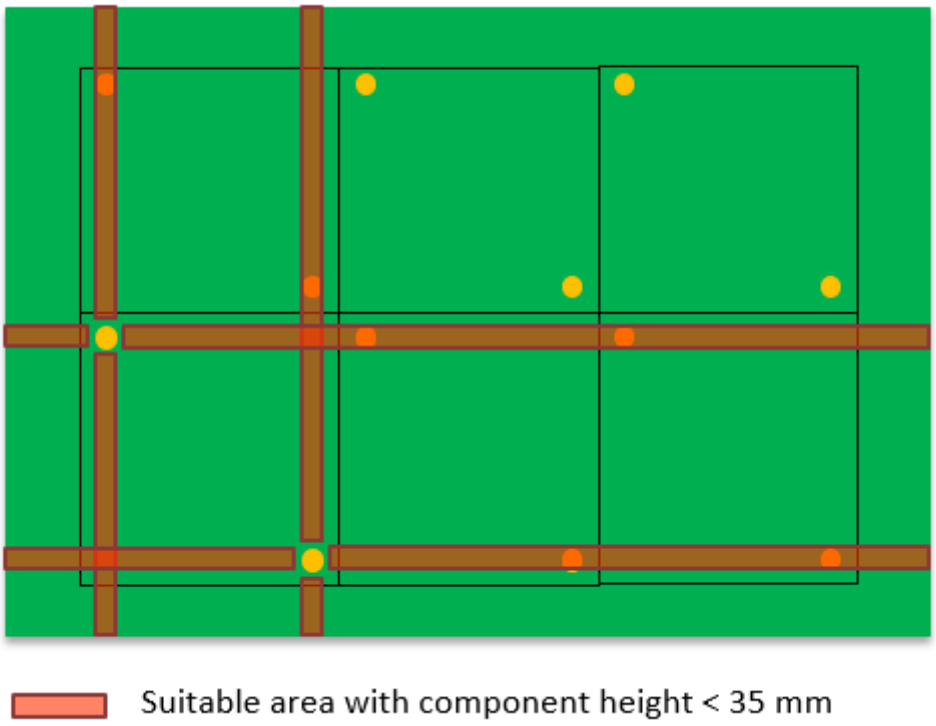
Picture 9 – Fiducial position on the panel of board

- **Geometry**

  Refer to the Fiducial chapter.

3.1.2 Fiducial Area

To make a fiducial accessible for the camera, for any direction of insertion in the test area, it is suggested to respect the areas free of components with height ⩾ 35mm as shown in the figure.



Picture 10 – Free fiducial area

3.2 Fiducial for board presence check

The FP uses a series of reference points to detect if the board of the panel is mounted and consequently has to be tested.

Two types of such points exist:

1) **General panel fiducial (All Board Mark)**
   Used to determine if 1 or more boards on the panel are not mounted.

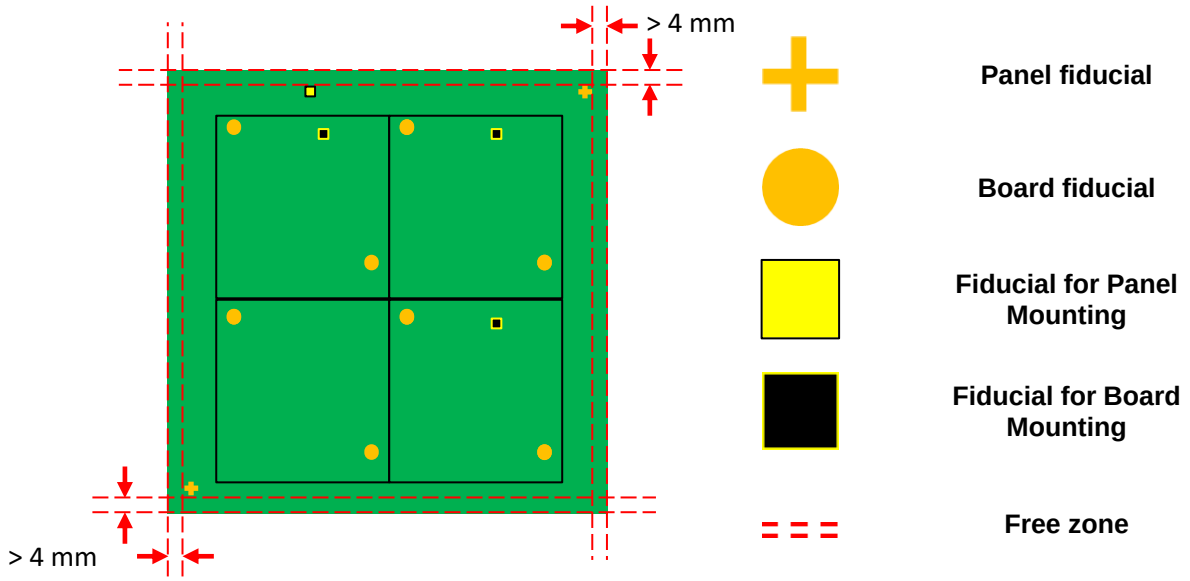
2) **Single board fiducial (Single Board Mark)**
   Used to determine if the board is mounted or not.

- **Use on FP**

	Status	Detection	Meaning	Following step
All board mark (A)	Covered	FAIL	1 or more boards are **not mounted**	Check the Single Board Mark
	Uncovered	PASS	All of the boards on panel are **mounted**	Execute TPGM on all boards
Single board mark (B)	Covered	FAIL	The board is **not mounted**	TPGM is not executed
	Uncovered	PASS	The board is **mounted**	Execute TPGM on the single board

Table 13 – Board detection according to fiducial used

- **Position**



Picture 11 – Examples of fiducials on a panel of boards

- **Geometry**

  Refer to the Fiducial chapter.

Designing fiducials to check the mounting of the boards simplifies the debug operations and saves time during the TPGM development.

3.3 Transportability

The shape of the board determines the side used to transport it in the testing machine.

For boards with unusual shape, it is advisable to provide devise methods to simplify transportability in the test equipment.

- **Characteristics**

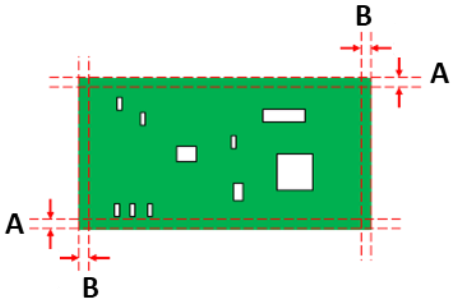
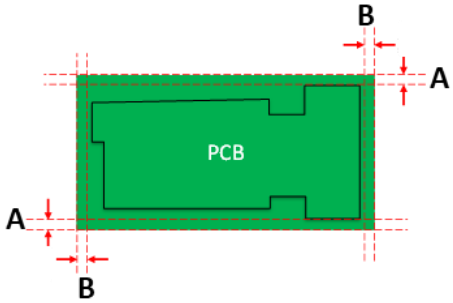
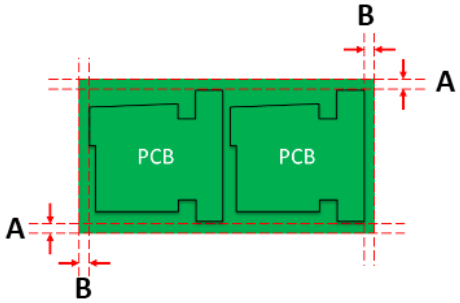
Board Typology	Layout	Area without components A	Area without components B
Regularly shaped		≥ 4 mm	≥ 4 mm
Irregularly-shaped		≥ 4 mm	≥ 4 mm
Panel of boards		≥ 4 mm	≥ 4 mm

Table 14 – Transportability and shape of the board

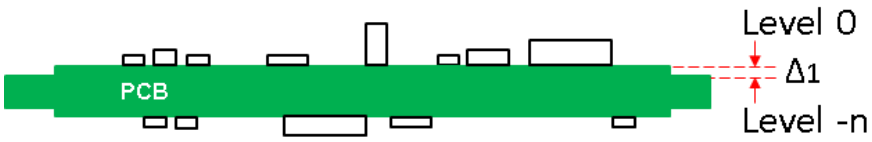
- **Transport of non-transportable board or panel**

  It is still possible to transport boards not designed according to the recommendations in this chapter with the resulting setup costs.
  The following is an example of a transport tray:

Picture 12 – Example of transport tray

- **Transport of board with uneven PCB level**

  The *Level 0* of the PCB corresponds to the surface where the probes will touch.
  If the card PCB level is uneven in the zone used to clamp it in the test area.
  It will still be possible to test it by applying suitable precautions in the test program.
  Nevertheless, where possible, fill the Δ1 gap to reduce the development time of the program.



Picture 13 – Side view of a board with uneven PCB level

3.4 Board dimension

The board testability on Flying probe system is based on the following characteristics:

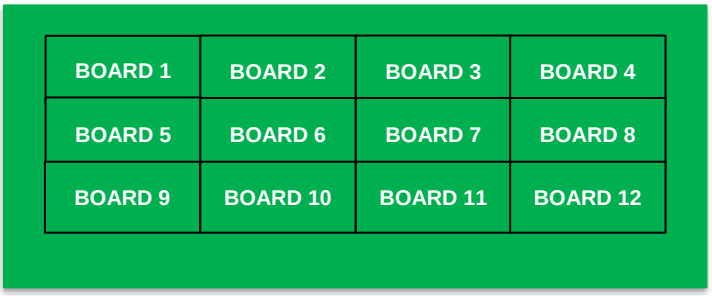
- **Operating Test Area**
  Work area of the FP tools installed on axes.

- **Board Clamp Area**
  Area for the clamping of the board in the test area.

Refer to the datasheet of own system to know maximum operating areas.

3.5 Panel of boards

Panel of boards include more boards and are the best practice to optimize their assembly and test times.
The FP is able to manage the test on both single boards and panel of boards.
The following table reports the main data:



Picture 14 – Example of a panel of boards

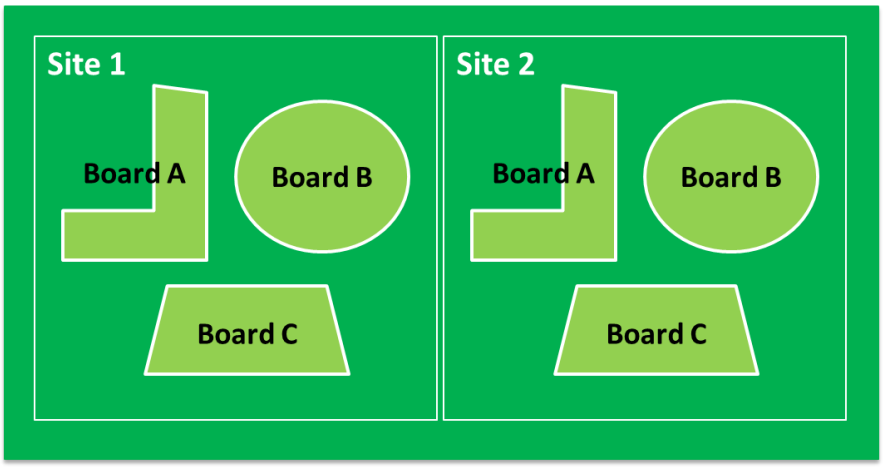
Characteristic	Notes
Max manageable number of boards per panel	256
Rotation management between boards	Yes
Top/bottom rotation management between boards	Yes
Manageable angles of rotation between boards	0-360°
Board fiducials	Required
Panel fiducials	Optional
Single board mark for board presence check	Optional

Table 15 – Panel of boards characteristics

A panel of boards allows saving on the setup time compared with a single UUT.
Consequently, the throughput per hour increases.

- **Different Part Numbers on panel of boards**

  To optimize test time, it is possible arrange different boards (with different Part Numbers) on a single panel.
  The boards in the following example will be tested using three different test program carried out in sequence.



Picture 15 – Panel of two boards with different Part Numbers

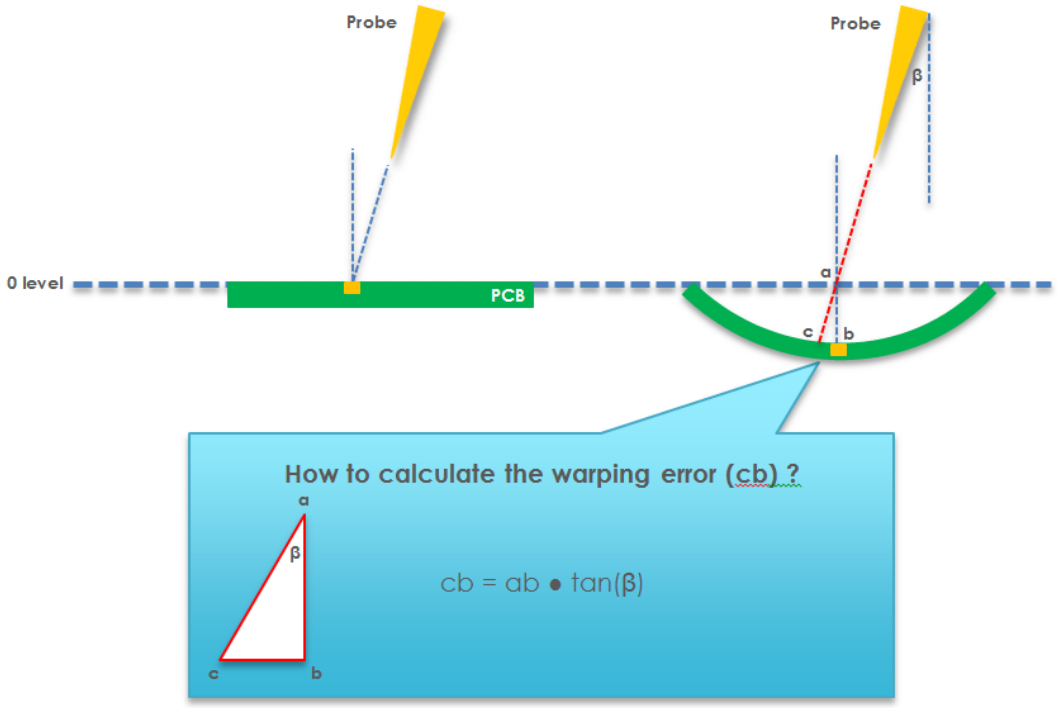
A panel of boards saves on tooling time compared to a single UUT. Consequently, the hourly throughput increases.

3.6 Warped boards

The FP its able to compensate the Z probes travel on the PCB level.

The compensantion its possible by the **Laser tool**.

Anyway take into account the board warping which could unpredictably affect the contact point as shown below:



Picture 16 – Warping error calculation

- **Warpage reduction**

  The following table shows some examples of precautions to limit the warping of the panel:

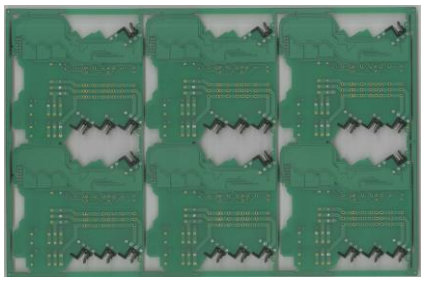
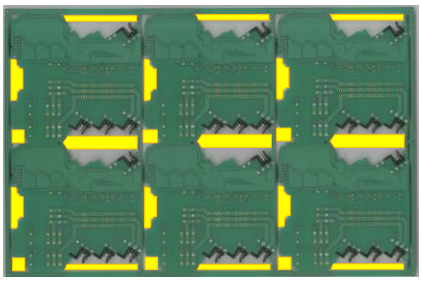
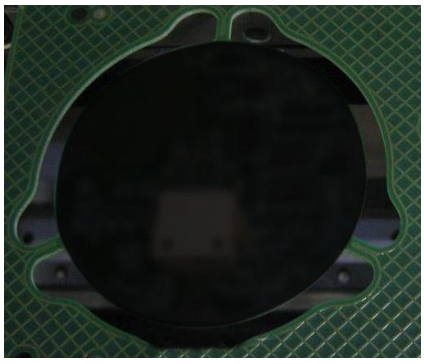
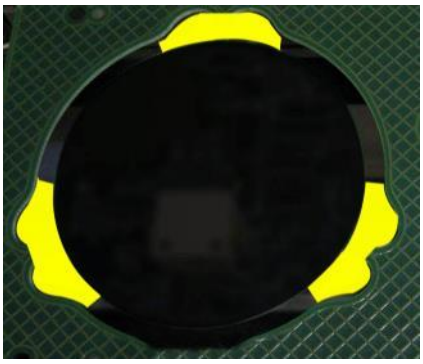
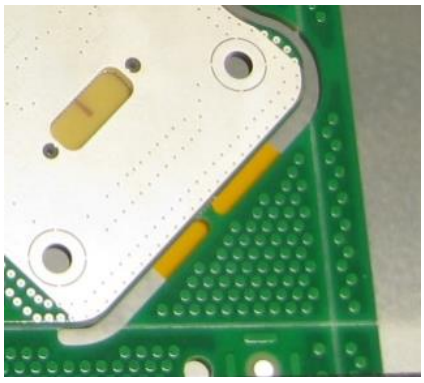
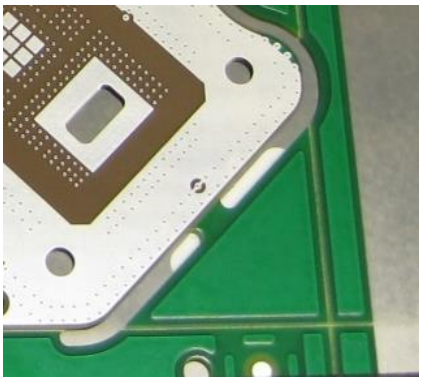
No.	Warpage risk	Warpage reduction
1	• Small tabs 	• Wider tabs 
2	• Small tabs 	• Wider tabs 
3	• Small tabs • Small surface to dissipate welding-related heat (PCB deformation effect) 	• Wider tabs • Increased surface to dissipate welding-related heat (PCB deformation reduction) 

Table 16 - Warpage reduction

- **Support frame for flexible boards**

  In case of particularly thin and / or flexible boards, the warping can be compensated by suitable supporting pallet that will affect the cost of testing.

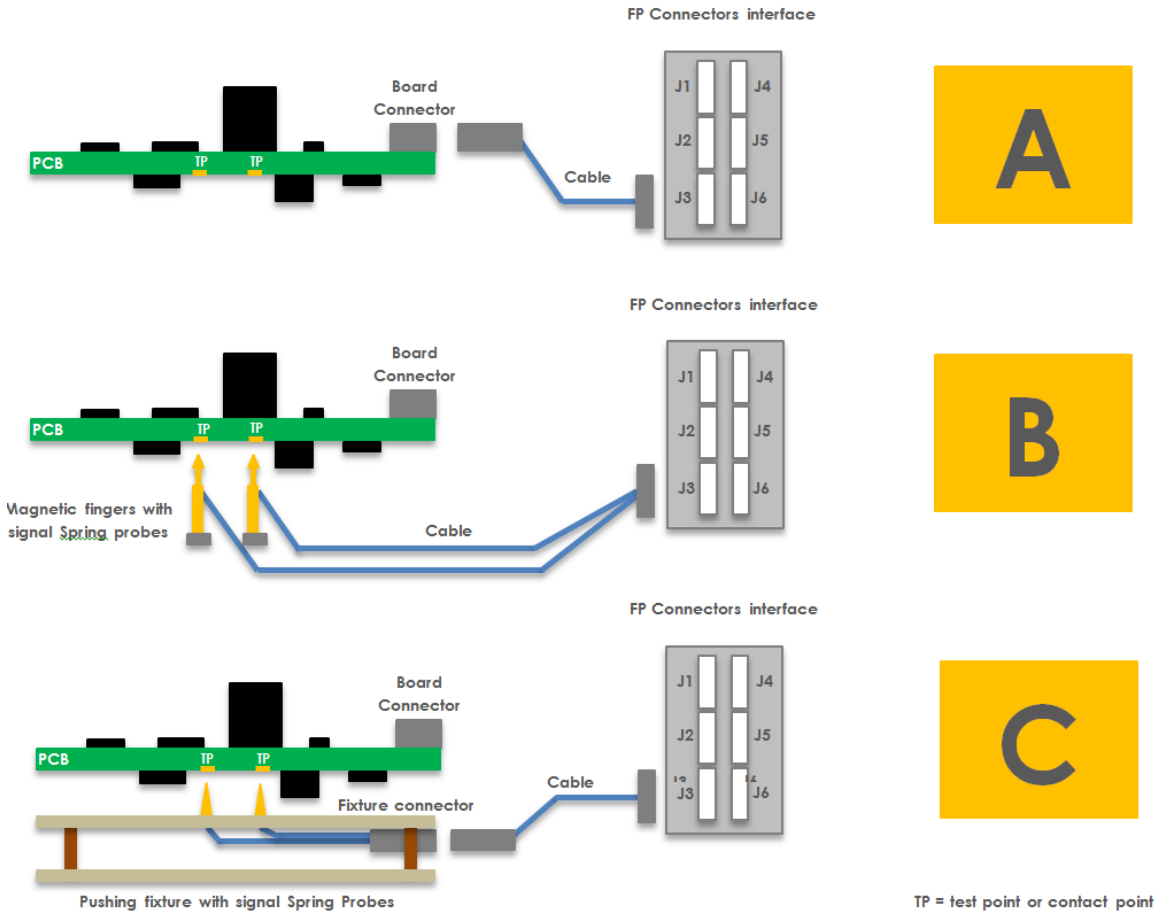
Picture 17 – Support frame for a flexible board

By designing the board to reduce warping, the cost of setup to increase rigidity is reduced.

4. Design rules to enhance test performance

4.1 Fixturing and wiring Series 1 and Series 2 systems

During the board design process it is possible to arrange the use of stimuli through connector interface instead flying probes to enhance the performance of the test.
The contact points to be touched by those stimuli have to be designed ad-hoc according to the test system used.
The following picture shows some typical solutions adopted.



Picture 18 – Typical solutions in using external resources

- **Characteristics of the board according to test solution**

Characteristic	Solution A Cabling	Solution B Fingers from the bottom side	Solution C Fixture
Applicability on In-Line systems	Yes (1)	Yes (3)	Yes (3)
Applicability on Manual systems	Yes	Yes	Yes
Applicability on single boards	Yes	Yes	Yes
Applicability on panels of boards	Yes (2)	Yes (2)	Yes
Contact point minimum diameter	-	1.5mm	0.8mm
Contacts distribution	-	Uniform	Uniform
Minimum ideal center to center distance between contact points	-	24mm	2.54mm (100mils)
Minimum center to center distance between contact points	-	24mm	1.27mm (50mils)
UUT tooling holes required	-	-	2
Minimum tooling holes diameter	-	-	3mm
Cost of setup	Low	Average	High
Interval of setup on system	At each test	Once, at production start-up	Once, at production start-up

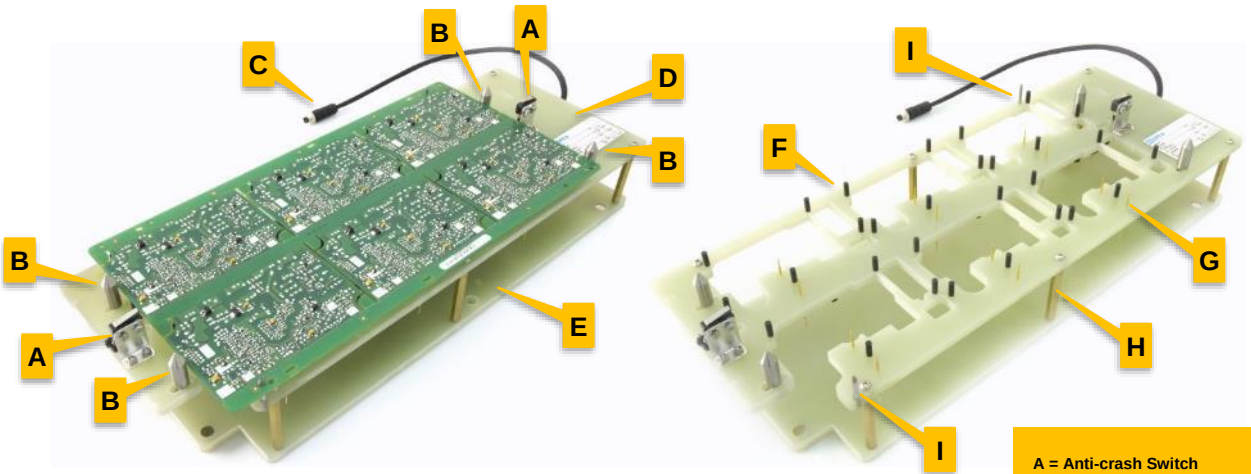
(1) RSL (Removable Shuttle Loader) required
(2) To check according to the kind of test to be executed on the UUT
(3) 4 axes system only

Table 17 – Characteristics of the board according to test solution

4.1.1 Fixturing on panel of boards

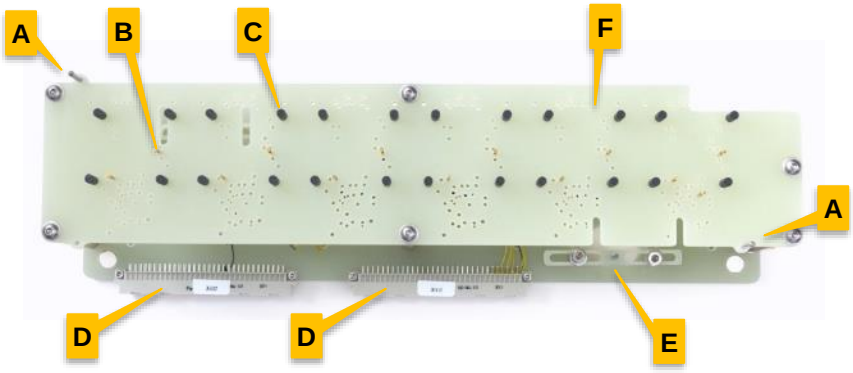
The fixture is a tool to enhance the test performance on 4-probe systems.

- **Parts of the fixture**



A = Anti-crash Switch
B = Reference pins
C = Anti-crash cable
D = Fixture top layer
E = Fixture bottom layer
F = UUT Stand-offs
G = Signal spring probes
H = FP floor-fixture spacers
I = Centering pins

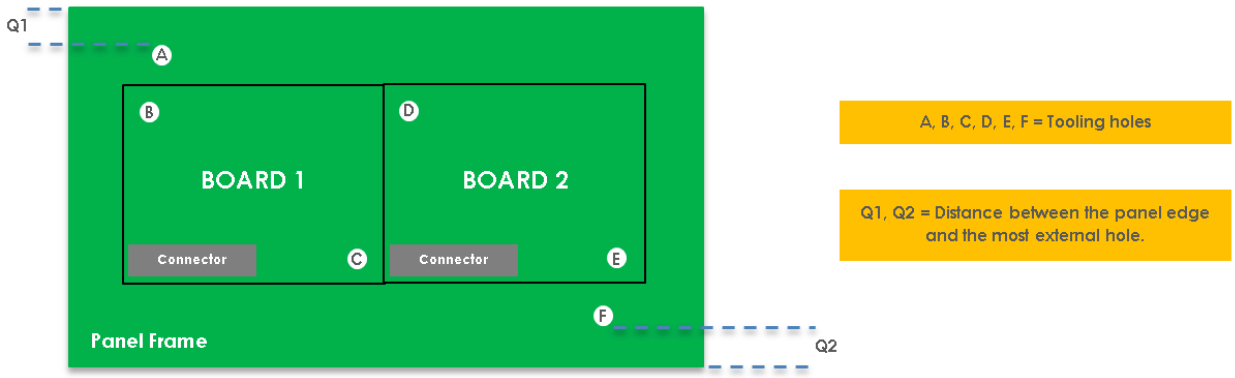
Picture 19 – Example of a 6-board panel fixture for an In-Line system



A = Centering pins
B = Signal spring probes
C = UUT Stand-offs
D = Feedback connector to FP interface
E = Fixture bottom layer
F = Fixture top layer

Picture 20 – Example of a 6-board panel fixture for a Manual system

4.1.1.1 Mechanical characteristics for panel centering



Picture 21 – Example of a 2-board panel to be tested using a fixture

Characteristic	Test system model			
	Shuttle Loader	**Manual**	**In-Line**	**Back Panel**
Min diameter A, B, C, D, E, F	2mm	2mm	3mm	3mm
Minimum Q1, Q2 if used for tooling	1mm	1mm	7.5mm	7.5mm
Test points distribution on the bottom	uniform			

(1) Do not concentrate the test points on a specific area of the UUT to avoid bending it with the push of the spring probes on the bottom side.

Table 18 – Mechanical characteristics for panel centering

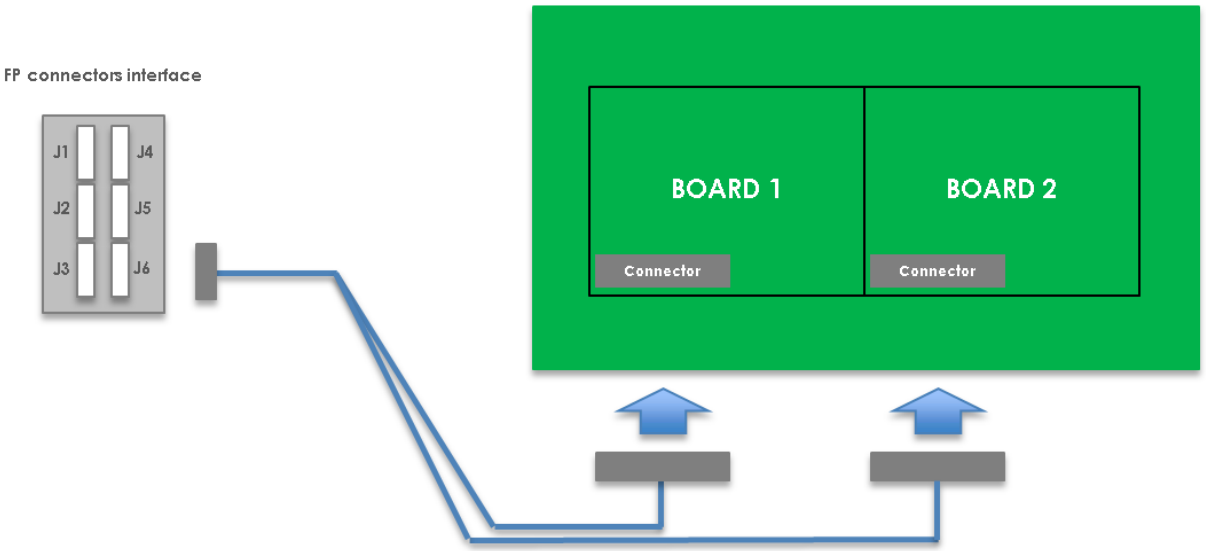
If the UUT mechanical references are suitably designed, it will be possible to save the hours of work necessary for the arranging of particular setups due to the noncompliance with the quotes specified on table.

4.1.2 Cabling on panel of boards

Cabling is a tool to enhance the test performance on Flying Probe systems.

When arranging a setup as shown in picture, it is recommended to place the connectors of the external cable according to the following rules:

1) On the side with less or none accessibility to the copper tracks (so that the test with FP probes is executed on the opposite side).
2) As close as possible to the border of the UUT, in order to avoid the passage of the cable over the components (if the connector is on the same side used for the test).



Picture 22 – Example of setup through cable on a panel of boards

The table below reports the applicability of the solution with cabling on panel of boards sorted by model of system:

Characteristic	Test system model\			
	Shuttle Loader	**Manual**	**In-Line**	**Back Panel**
Applicability of cabling on panel of boards	Yes	Yes	Yes (1)	Yes \(1)

(1) RSL (Removable Shuttle Loader) required if available on system tester.

Table 19 – Cabling applicability per system model

€ Setup through cabling is usually less expensive than a fixture.

4.2 Open pin test

The SPEA FP is able to check the components pins welding through a 2 different techniques known as:

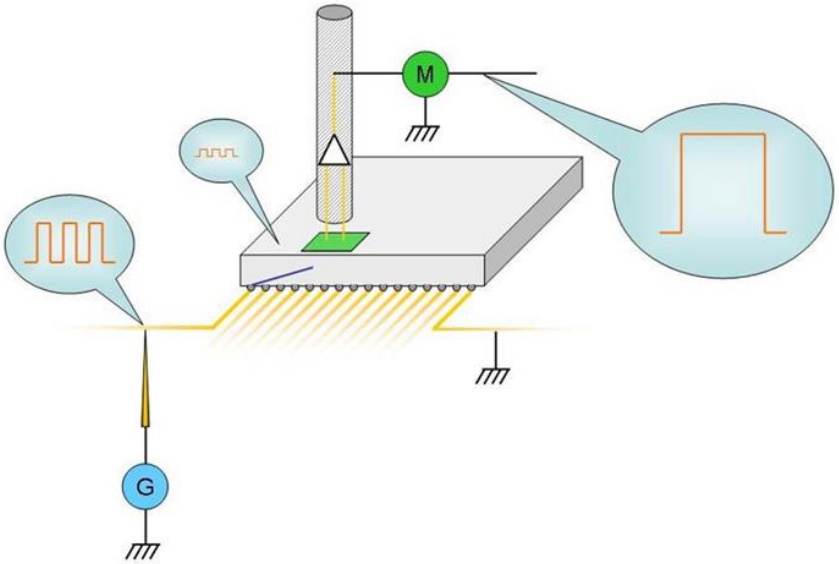
1. Electro scan
2. Junction scan

4.2.1 Electro scan

The test consists in forcing a signal on the net of the pin under test with a probe; then, with a specific hardware, the electric field emitted by the pin itself is measured through the case of the component under test.

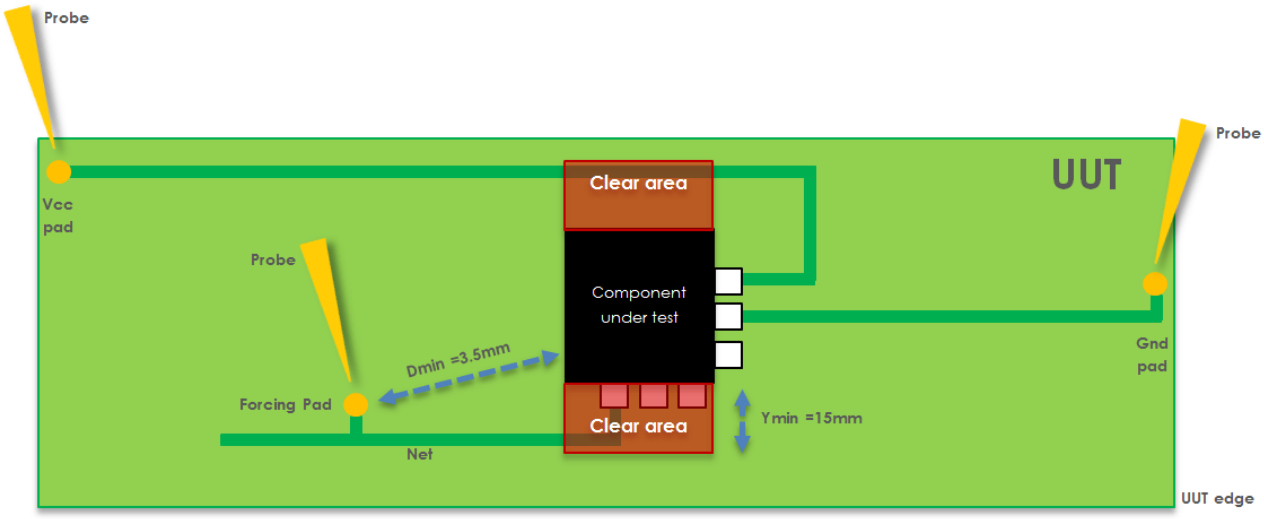
Below, a representation of the test technique.

- **Test technique**



Picture 23 – Electro scan Test technique

- **Accessibility of the nets connected to the pin under test**



Picture 24 – Accessibility of the nets connected to the pin under test

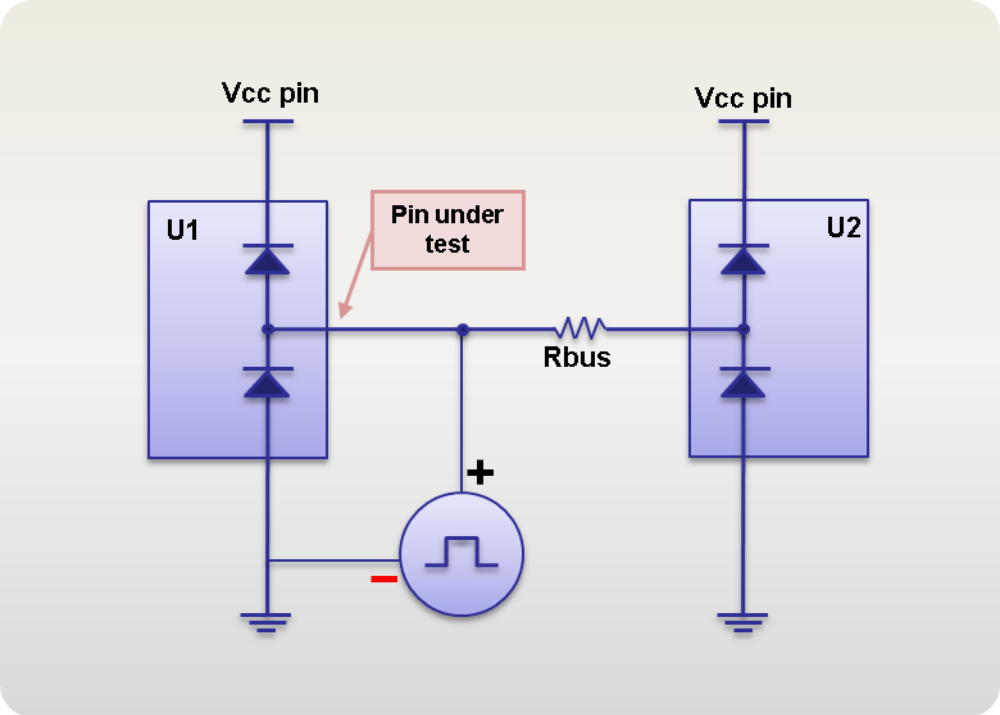
Characteristic	Parameter	Value
Min. distance between the forcing pad to the case of the component	D min	3.5 mm
Clear area suggested where the components height ≤ 7mm	Y min	15 mm
Component power net accessibility suggested	Vcc	Close to the UUT edge
Component ground net accessibility suggested	GND	Close to the UUT edge

Table 20 – Test point accessibility

4.2.2 Junction scan

The Junction Scan is the testing technique that verifies the welding of the pin by measuring the component diodes (also called clamp diodes).

Where possible, in compliance with the electrical functionality of the board, it is advisable to provide separation resistors on the connection bus (called Rbus) between two components in order to be able to individually test the clamp diode avoiding the parallel effect.



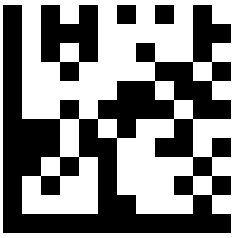
Picture 25 - Junction Scan working principle

4.3 2D Code

The 2D Code is a two-dimensional bar code, i.e. matrix, composed of blacks modules arranged in a square pattern for storage of information such as:

- Serial Number
- Lot Number
- Manufacturing date
- ...

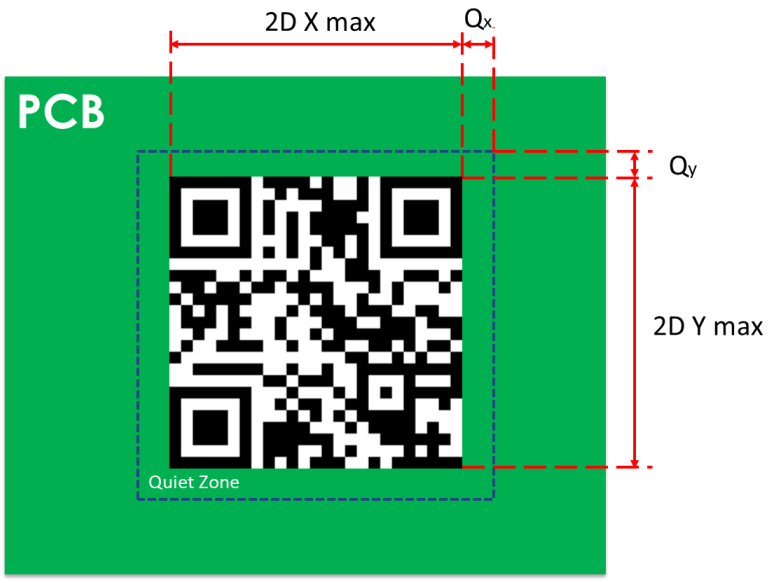
- **Formats**



DataMatrix

QR Code

- **Dimensions**



Picture 26 – QR code quotes

No.	Parameter	Dimension
1	2D Xmax	6 mm
2	2D Ymax	6 mm
3	Minimum Qy	1 mm
4	Minimum Qx	1 mm
5	Minimum Dot	150x150 µm

Table 21 – QR code dimensions

- **Other characteristics**

No.	Characteristic	Requirement
1	Not covered by the overlying components	MINIMUM
2	Positioned at least on the primary test side	MINIMUM (1)
3	Positioned on both sides of the board	RECOMMENDED (2)
4	Adjacent area free from other codes or labels	RECOMMENDED
5	High contrast image compared to PCB	MINIMUM

(1) On systems with 6 or 8 probes

(2) On systems with 4 probes

Table 22 – 2D Code characteristics

4.4 Multi Probe Unit (4080)

The Multi Probe Unit (MPU) is a mini flying fixture that can be installed on 4080 system:

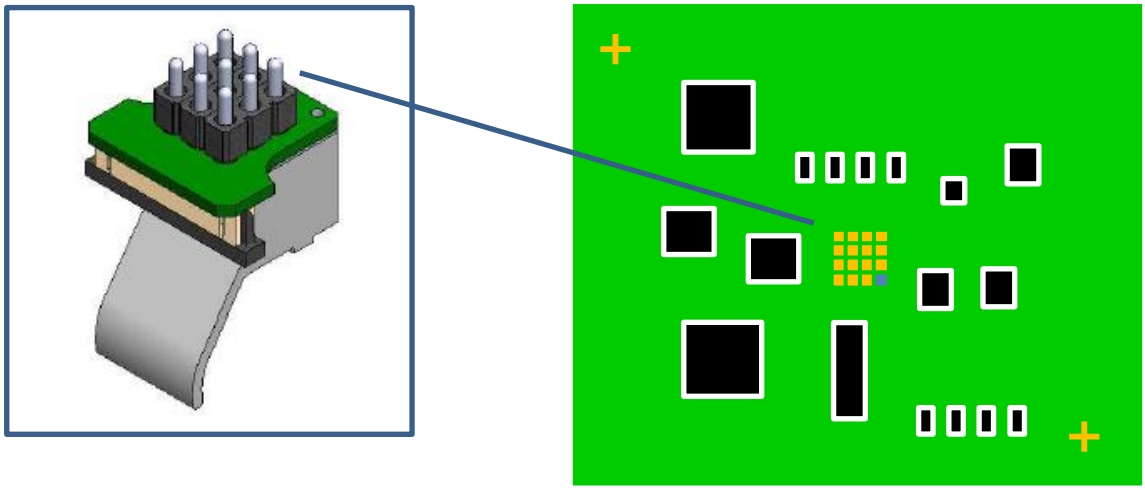
- Top side on axes 1 and 4
- Bottom side axis 5 and 8

It can contact a designed pad array of the UUT and its able to perform tests such as:

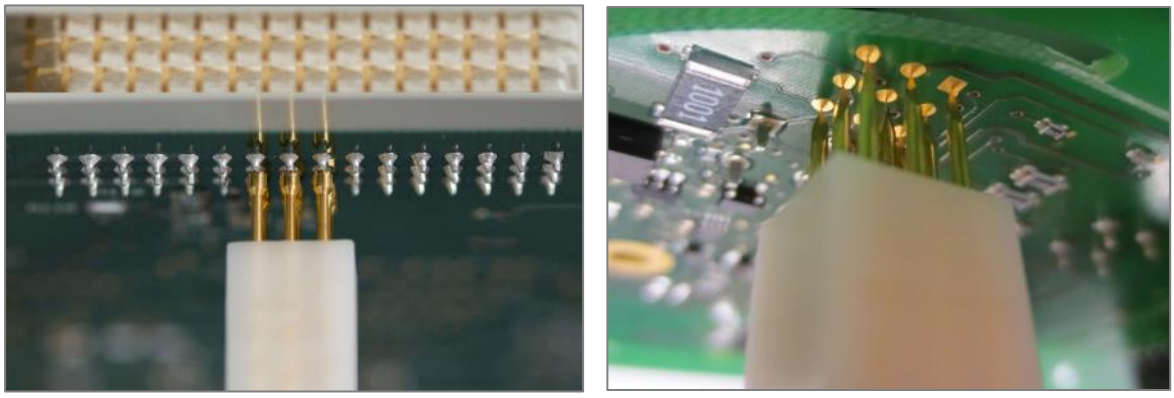
- Functional Test
- Boundary Scan
- Power-On Test

The information in this chapter is useful for **electronic designer** and **PCB designer** involved in the following aspects:

- Mechanical design of pads and PCBs
- Physical constraints of the area surrounding the MPU
- Positioning of the pads on the UUT
- Electrical connections



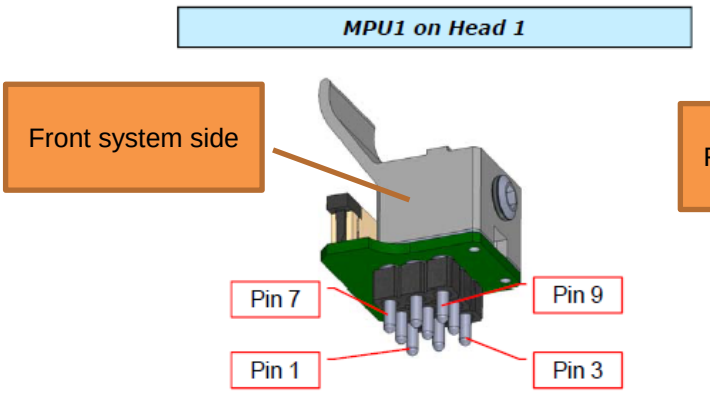
Picture 27 – Multi Probe Probe Unit (MPU) and UUT Pod Area



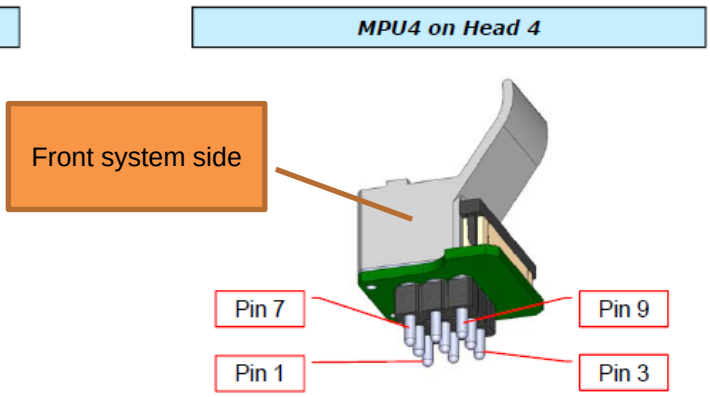
Picture 28 – Example of contact on connector VS dedicated pads

4.4.1 Multi Probe on system top side

4.4.1.1 Head 1- 4 pinout



MPU Head 1			
Pin No.	BSCAN Name	SPEA Name	ICT Signal
1	BS_TCK_1	MPU1 signal 1	Ch 193/194
2	BS_TMS_1	MPU1 signal 2	Ch 195/196
3	BS_TDI_1	MPU1 signal 3	Ch 197/198
4	BS_TDO_1	MPU1 signal 4	Ch 199/200
5	BS_/TRST_1	MPU1 signal 5	Ch 201/202
6	BS_GND_1	MPU1 signal 6	Ch 203/204
7	(Power1+)	MPU1 signal 7	Ch 205/206
8	(Power2+)	MPU1 signal 8	Ch 207/208
9	(PowerGnd)	MPU1 signal 9	Ch 209/210

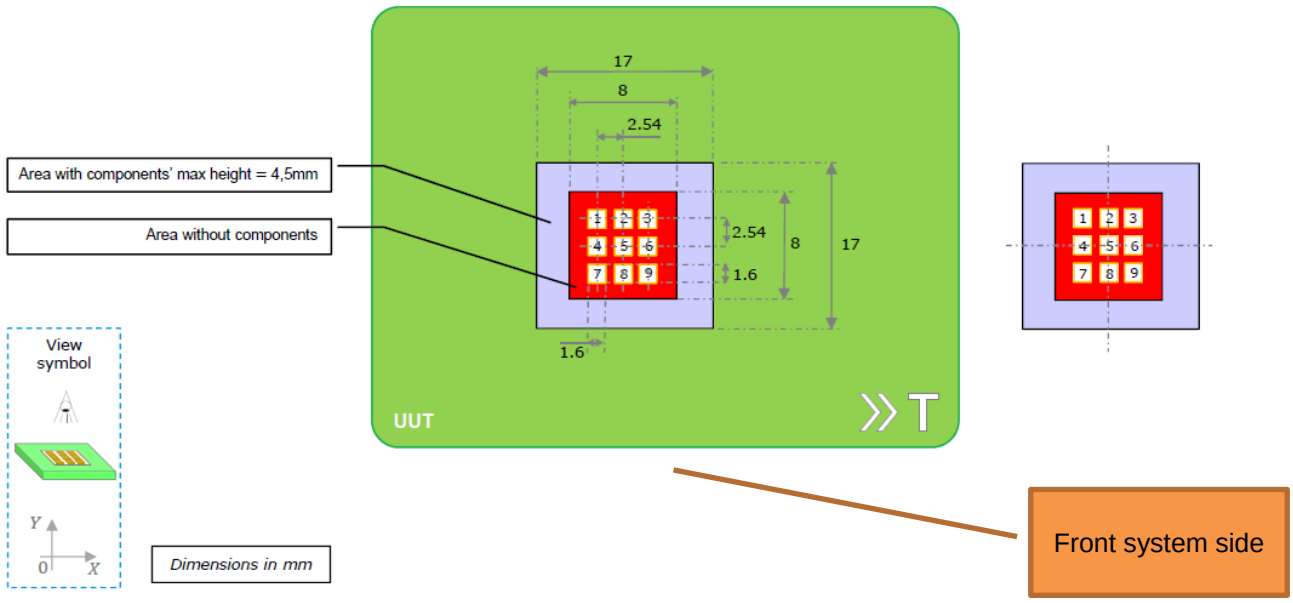


MPU Head 4			
Pin No.	BSCAN Name	SPEA Name	ICT Signal
1	BS_TCK_2	MPU4 signal 1	Ch 211/212
2	BS_TMS_2	MPU4 signal 2	Ch 213/214
3	BS_TDI_2	MPU4 signal 3	Ch 215/216
4	BS_TDO_2	MPU4 signal 4	Ch 217/218
5	BS_/TRST_2	MPU4 signal 5	Ch 219/220
6	BS_GND_2	MPU4 signal 6	Ch 221/222
7	(Power1+)	MPU4 signal 7	Ch 223/224
8	(Power2+)	MPU4 signal 8	Ch 225/226
9	(PowerGnd)	MPU4 signal 9	Ch 227/228

Picture 29 – Layout and pinout head 1 and 4

4.4.1.2 Pads design

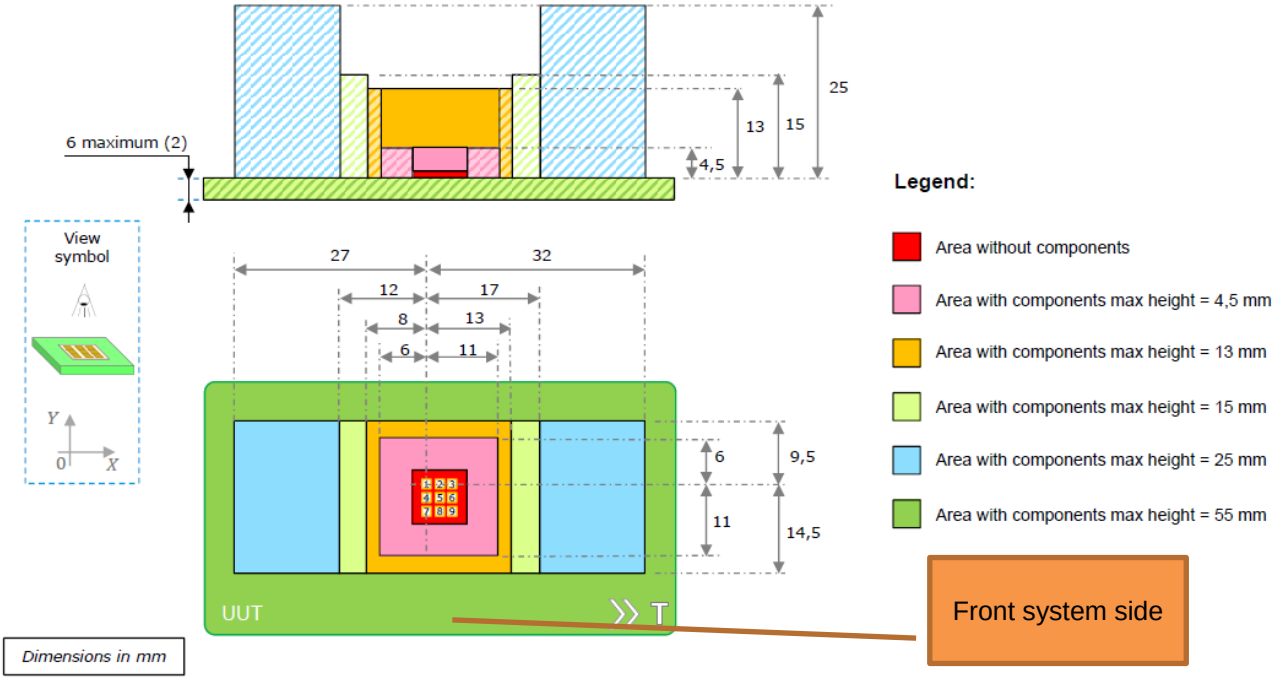
Each MPU pad is composed by 9 square pads with the layout described below.
NOTE 1: MPU pads must be placed on the board side to be contacted by System Top Heads.
NOTE 2: MPU pads must be on the board PCB.
NOTE 3: MPU heads cannot rotate, so pads layout and board positioning inside the Flying Probe test area are related.



Picture 30 – Pad dimensions and layout of MPU's 1 and 4 top Side [dimensions in mm]

4.4.1.3 Components height

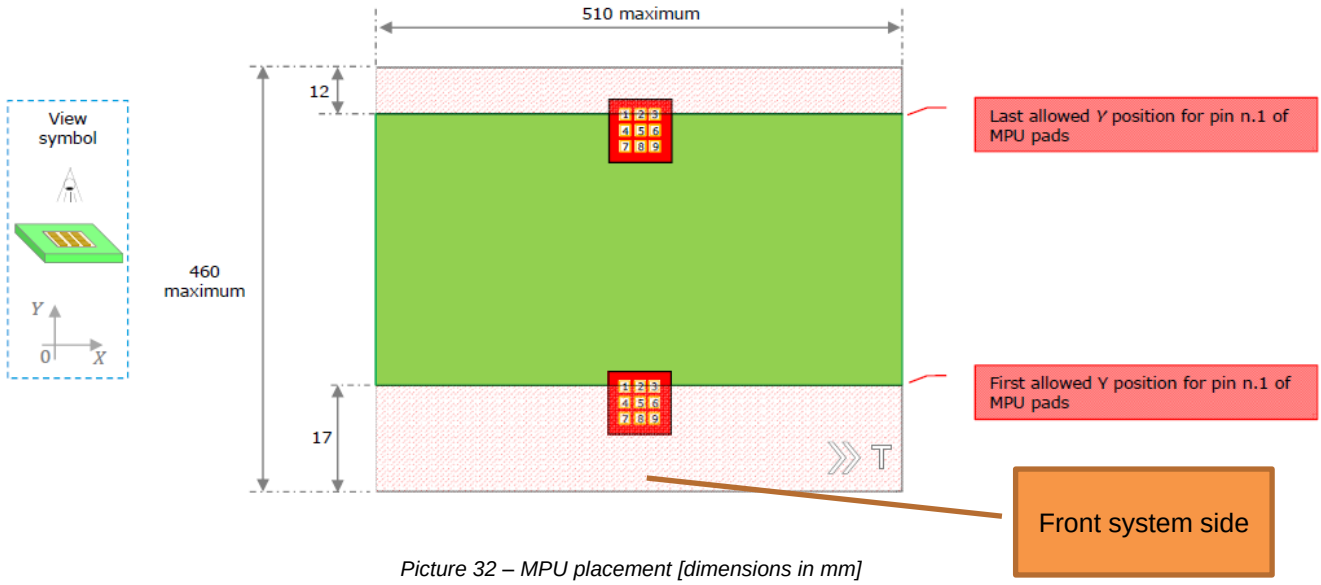
Around each MPU pad, components' height must respect conditions described below (1):



(1) When the MPU mechanism is not enabled it does not generate any restriction on components or on axes positioning capability
(2) It's possible to use MPUs only if the UUT thickness is lower than 6mm

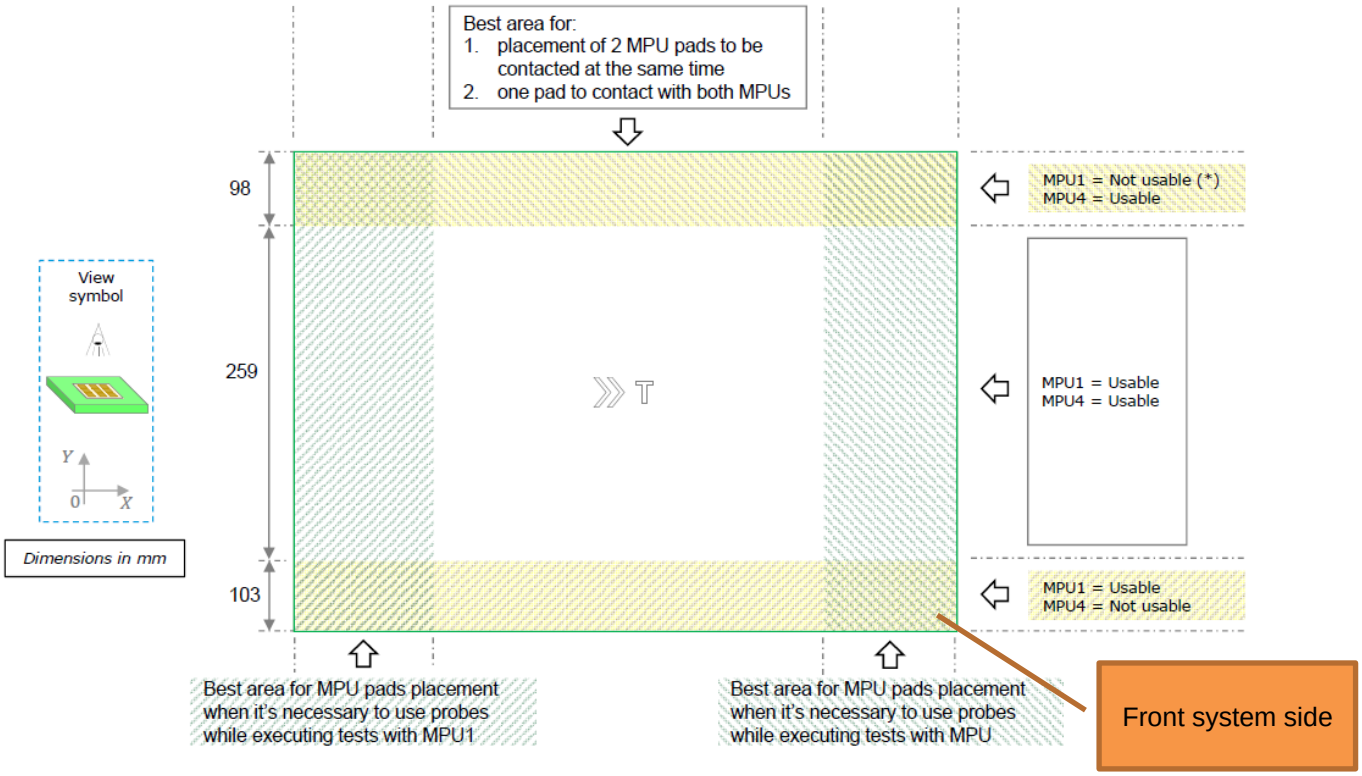
Picture 31 – Restriction components areas of MPU pads [dimensions in mm]

4.4.1.4 Working area



Picture 32 – MPU placement [dimensions in mm]

4.4.1.5 Placement inside UUT

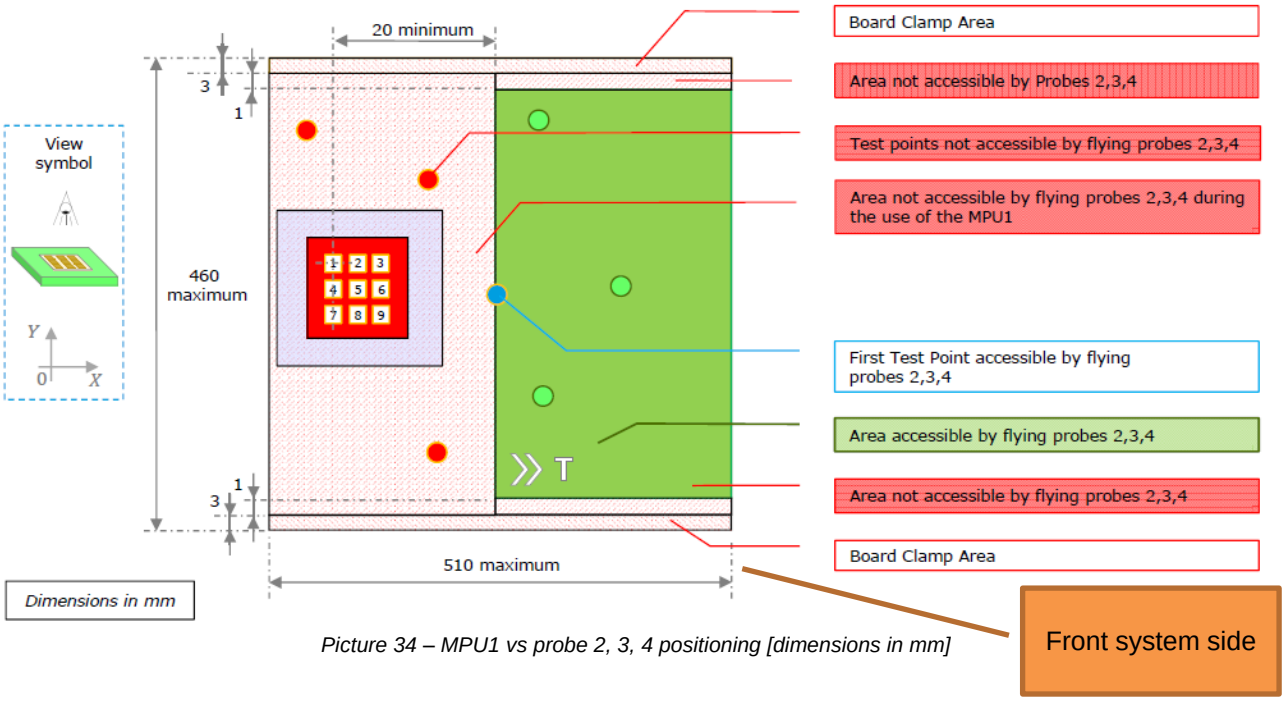


(*): MPU1 is not usable if UUT's depth is greater than 362mm (equal to 103mm+259mm).

Picture 33 – Suitable placement area inside UUT [dimensions in mm]

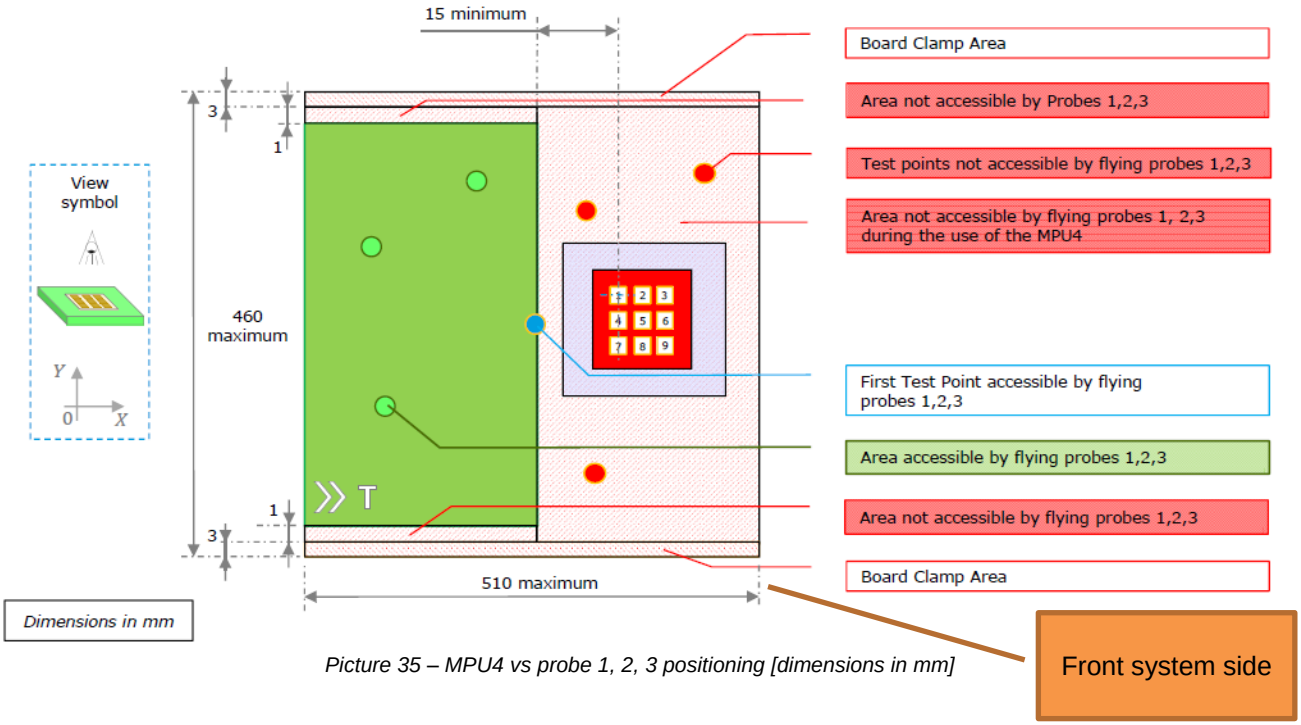
4.4.1.6 MPU vs other test points

Test points closer than 20mm in X coordinate from pin 1 of MPU pod to be contacted with **MPU1** can not be reached by any probe. Test points further than 20mm can be contacted by other axes probes while **MPU1** is contacting the MPU pod (Picture 34).



Picture 34 – MPU1 vs probe 2, 3, 4 positioning [dimensions in mm]

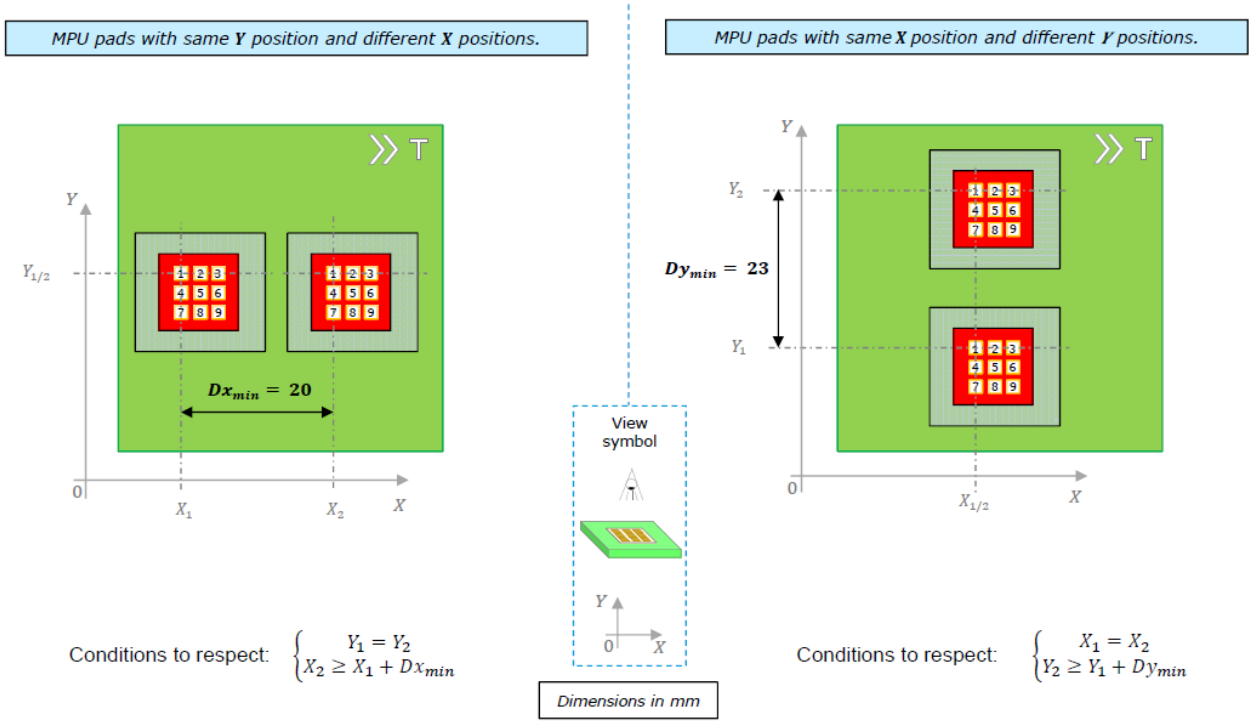
Test points closer than 15mm in X coordinate from pin 1 of MPU pod to be contacted with **MPU4** can not be reached by any probe. Test points further than 20mm can be contacted by other axes probes while **MPU4** is contacting the MPU pod (Picture 35).



Picture 35 – MPU4 vs probe 1, 2, 3 positioning [dimensions in mm]

4.4.1.7 Simultaneously MPU positioning

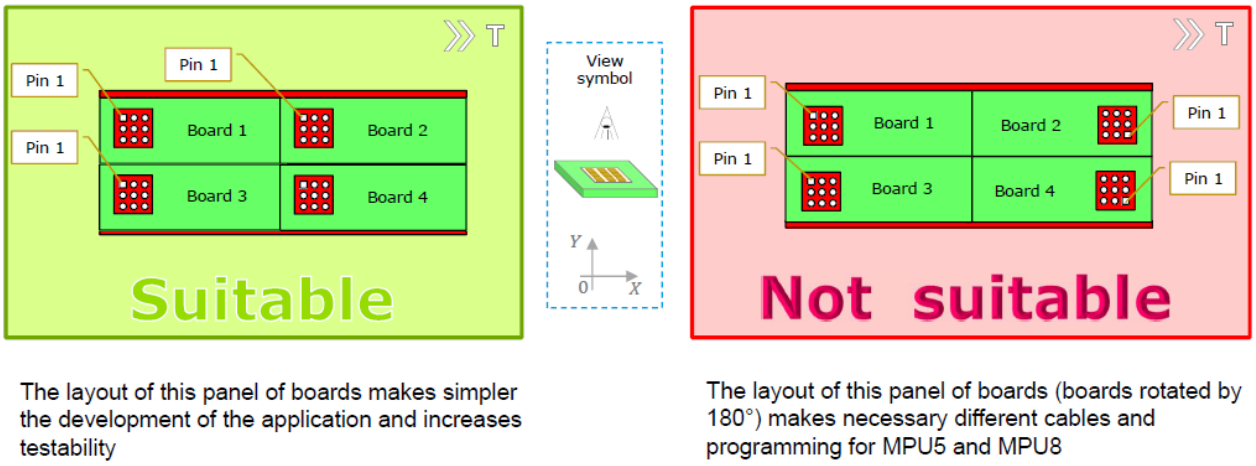
To utilize no.2 MPU simultaneously below condition must be respected.



Picture 36 – Minimum distance between 2 pods per MPU on the same board [dimensions in mm]

4.4.1.8 MPU on panel of boards

Positioning the MPU pods as shown in picture, the development of the program will be simplified.



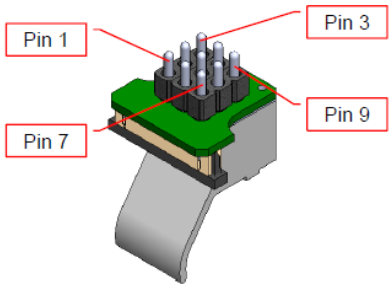
Picture 37 – Suitable and NOT suitable position on panel of boards [dimensions in mm]

4.4.2 Multi Probe on system bottom side

4.4.2.1 Head 5-8 pinout

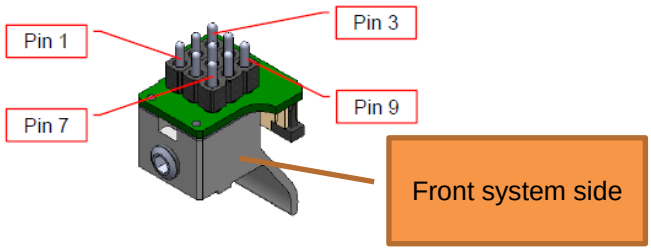
The MPU head is designed with 3 rows and 3 columns of pins with the following pinout:

MPU5 on Head 5



MPU Head 5			
Pin No.	BSCAN Name	SPEA Name	ICT Signal
1	BS_TCK_3	MPU5 signal 1	Ch 65/66
2	BS_TMS_3	MPU5 signal 2	Ch 67/68
3	BS_TDI_3	MPU5 signal 3	Ch 69/70
4	BS_TDO_3	MPU5 signal 4	Ch 71/72
5	BS_/TRST_3	MPU5 signal 5	Ch 73/74
6	BS_GND_3	MPU5 signal 6	Ch 75/76
7	(Power1+)	MPU5 signal 7	Ch 77/78
8	(Power2+)	MPU5 signal 8	Ch 79/80
9	(PowerGnd)	MPU5 signal 9	Ch 81/82

MPU8 on Head 8

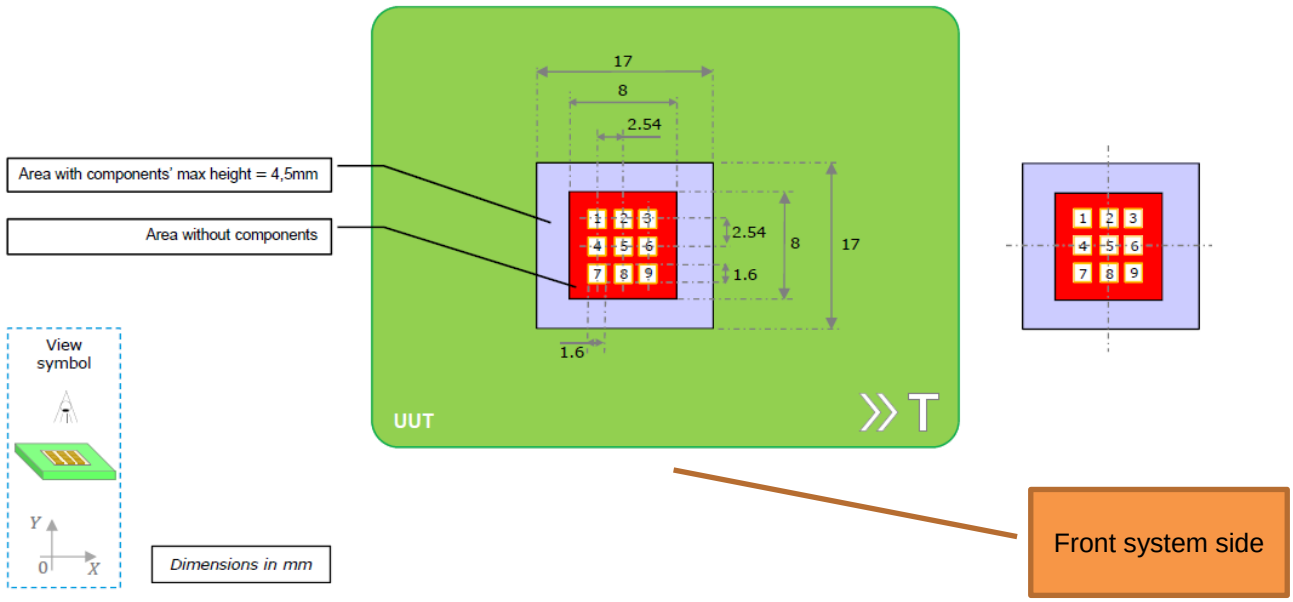


MPU Head 8			
Pin No.	BSCAN Name	SPEA Name	ICT Signal
1	BS_TCK_4	MPU8 signal 1	Ch 83/84
2	BS_TMS_4	MPU8 signal 2	Ch 85/86
3	BS_TDI_4	MPU8 signal 3	Ch 87/88
4	BS_TDO_4	MPU8 signal 4	Ch 89/90
5	BS_/TRST_4	MPU8 signal 5	Ch 91/92
6	BS_GND_4	MPU8 signal 6	Ch 93/94
7	(Power1+)	MPU8 signal 7	Ch 95/96
8	(Power2+)	MPU8 signal 8	Ch 97/98
9	(PowerGnd)	MPU8 signal 9	Ch 99/100

Picture 38 – Layout and pinout head 1 and 4

4.4.2.2 Pads design

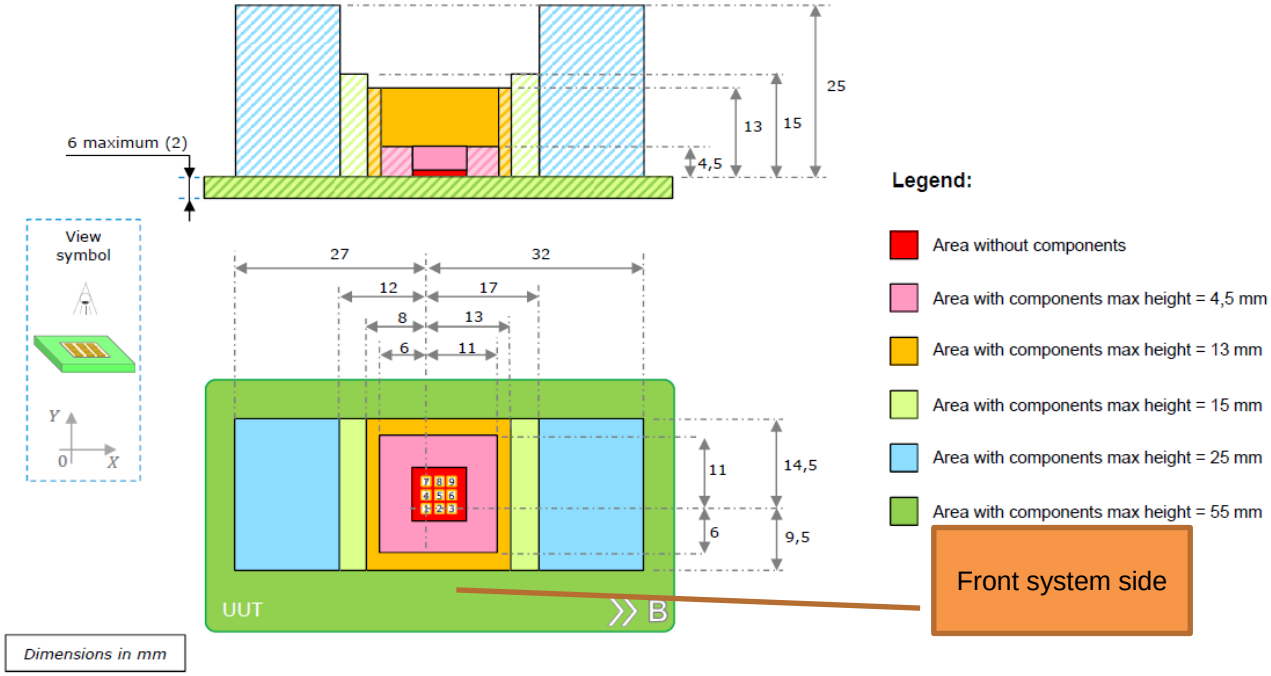
Each MPU pad is composed by 9 square pads with the layout described below.
NOTE 1: MPU pads must be placed on the board side to be contacted by System Top Heads.
NOTE 2: MPU pads must be on the board PCB.
NOTE 3: MPU heads cannot rotate, so pads layout and board positioning inside the Flying Probe test area are related.



Picture 39 – Pad dimensions and layout of MPU's 1 and 4 top Side [dimensions in mm]

4.4.2.3 Components height

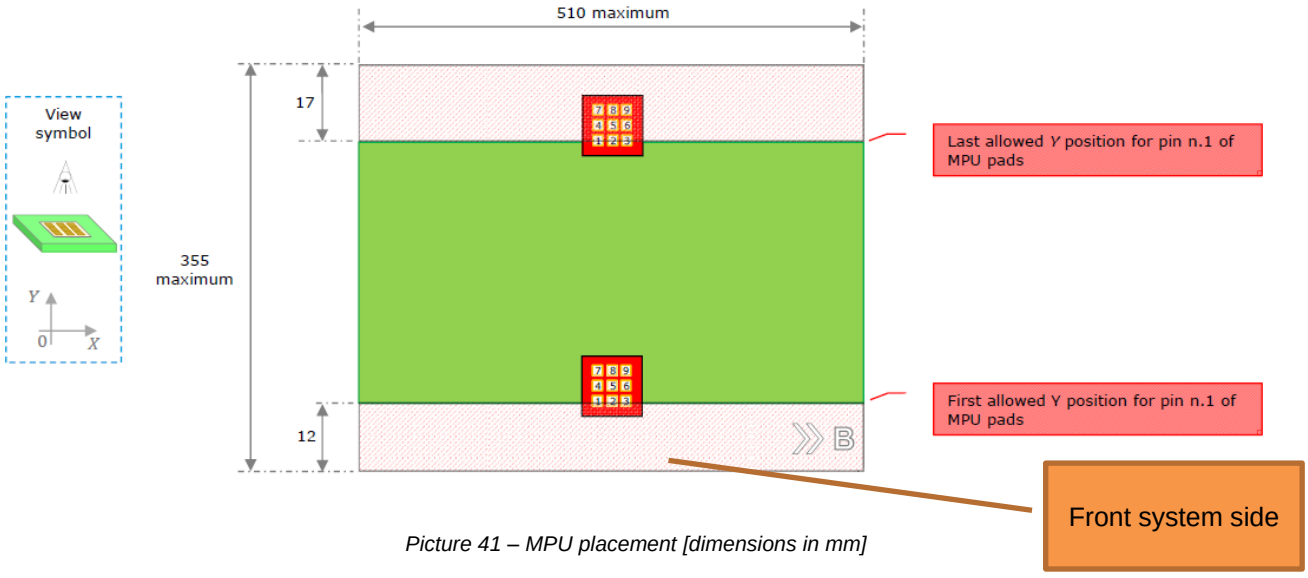
Around each MPU pad, components' height must respect conditions described below (1):



(1) When the MPU mechanism is not enabled it does not generate any restriction on components or on axes positioning capability
(2) It's possible to use MPUs only if the UUT thickness is lower than 6mm

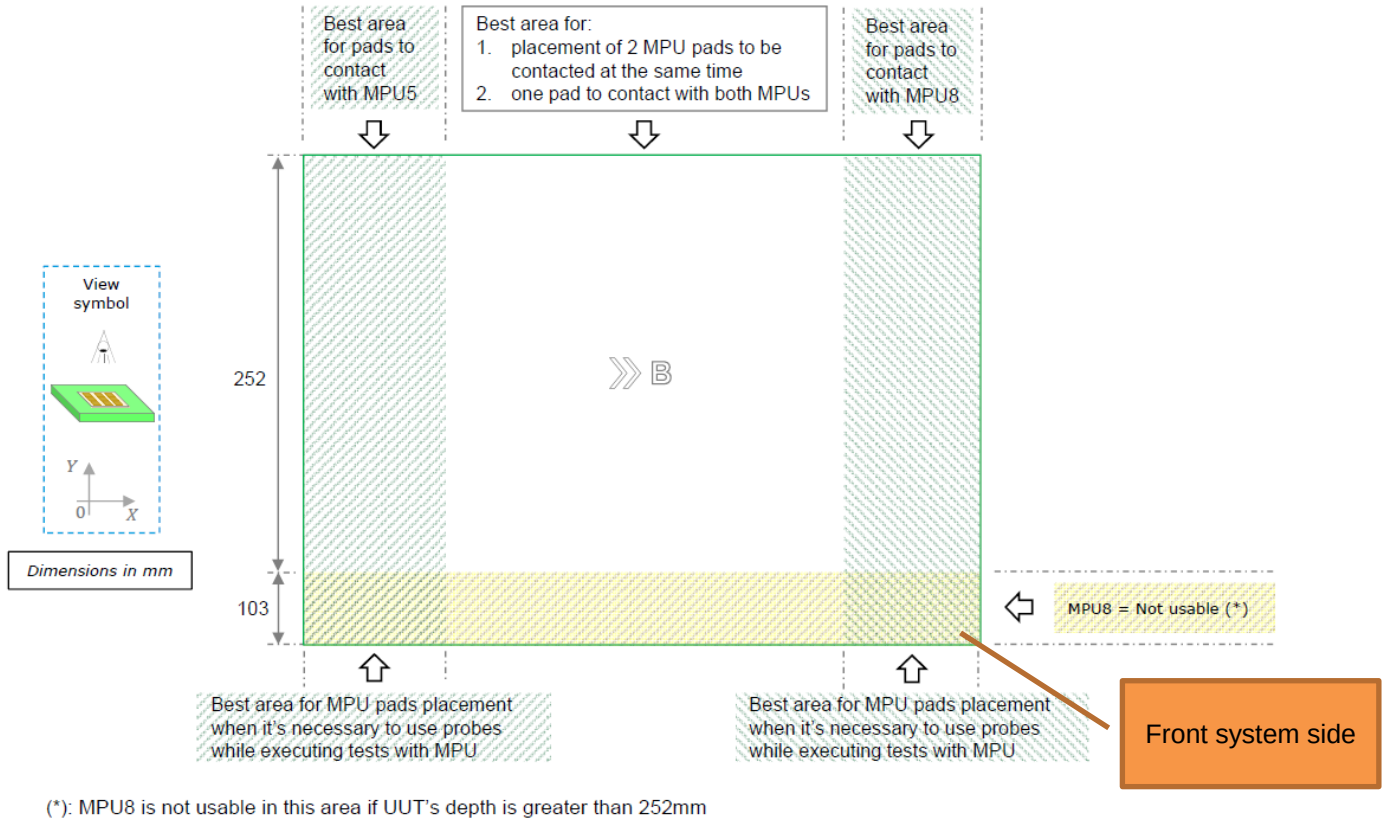
Picture 40 – Restriction components areas of MPU pads [dimensions in mm]

4.4.2.4 Working area



Picture 41 – MPU placement [dimensions in mm]

4.4.2.5 Placement inside UUT

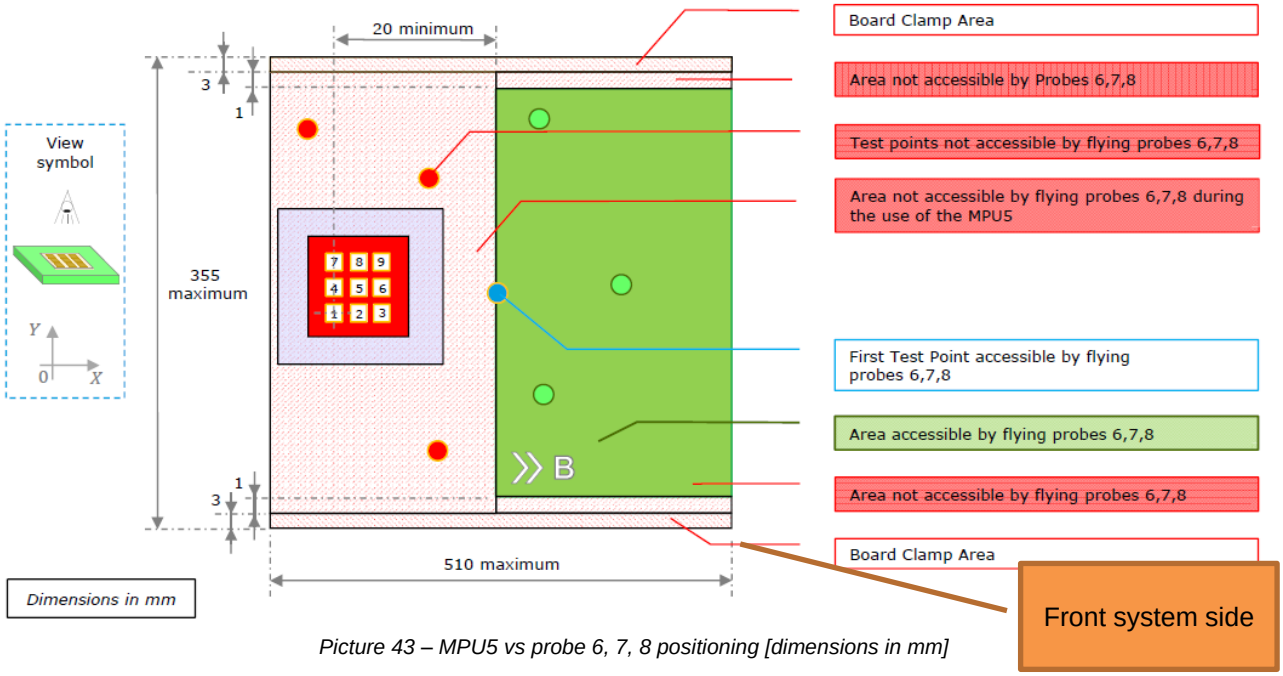


(*): MPU8 is not usable in this area if UUT's depth is greater than 252mm

Picture 42 – Suitable placement area inside UUT [dimensions in mm]

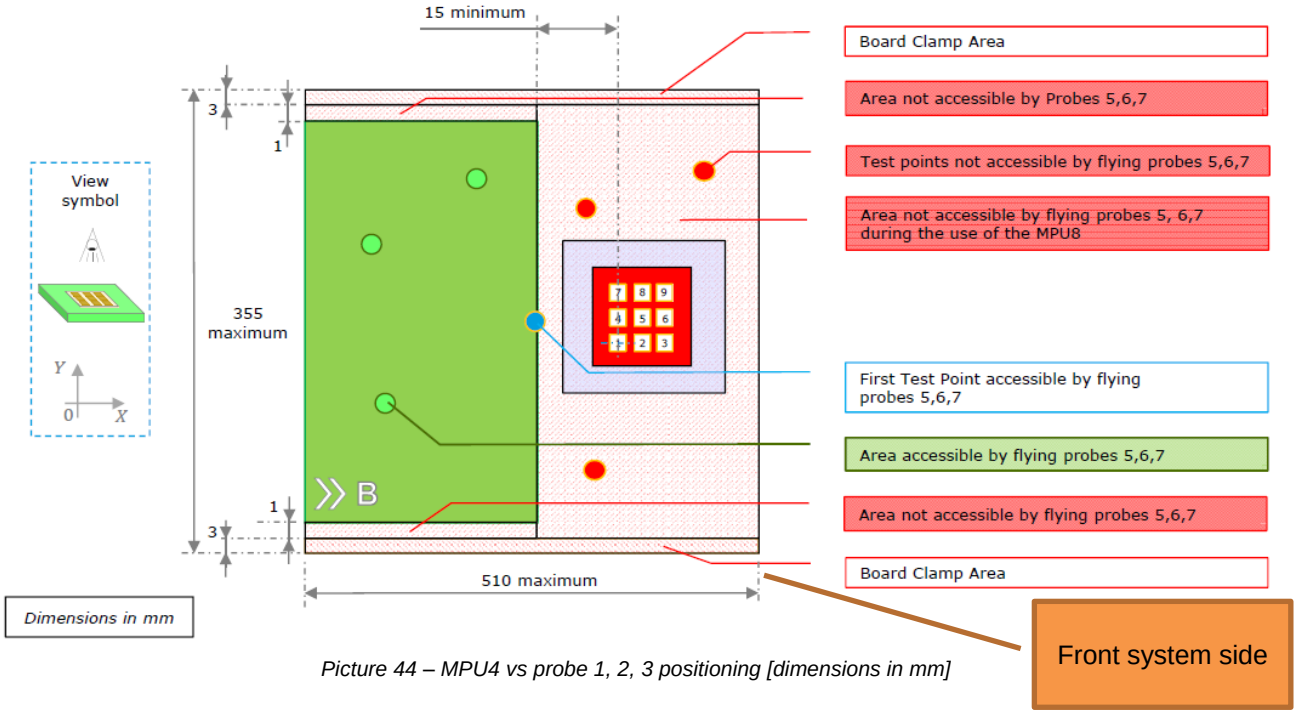
4.4.2.6 MPU vs other test points

Test points closer than 20mm in X coordinate from pin 1 of MPU pod to be contacted with **MPU5** can not be reached by any probe. Test points further than 20mm can be contacted by other axes probes while **MPU5** is contacting the MPU pod (Picture 43).



Picture 43 – MPU5 vs probe 6, 7, 8 positioning [dimensions in mm]

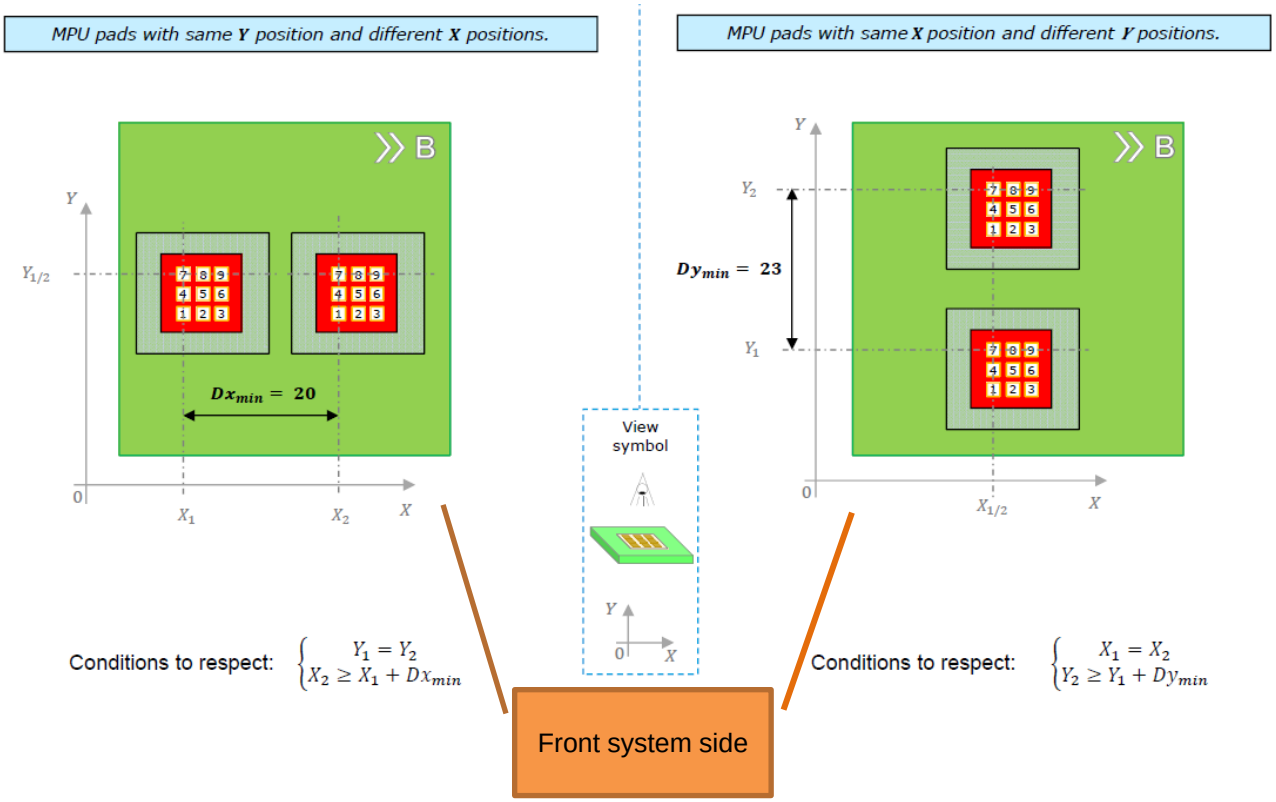
Test points closer than 15mm in X coordinate from pin 1 of MPU pod to be contacted with **MPU8** can not be reached by any probe. Test points further than 20mm can be contacted by other axes probes while **MPU84** is contacting the MPU pod (Picture 44).



Picture 44 – MPU4 vs probe 1, 2, 3 positioning [dimensions in mm]

4.4.2.7 Simultaneously MPU positioning

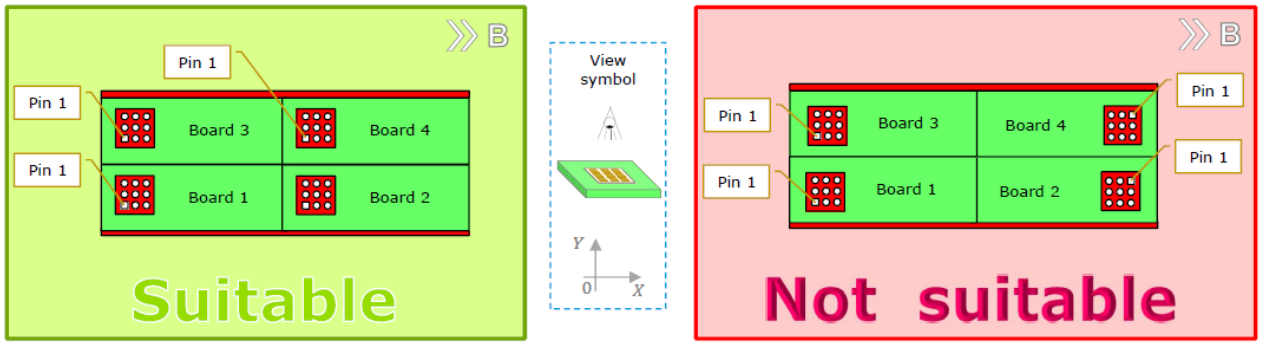
To use both MPU simultaneously below condition must be respected.



Picture 45 – Minimum distance between 2 pods per MPU on the same board [dimensions in mm]

4.4.2.8 MPU on panel of boards

Positioning the MPU pods as shown in picture, the development of the program will be simplified.



The layout of this panel of boards makes simpler the development of the application and increases testability

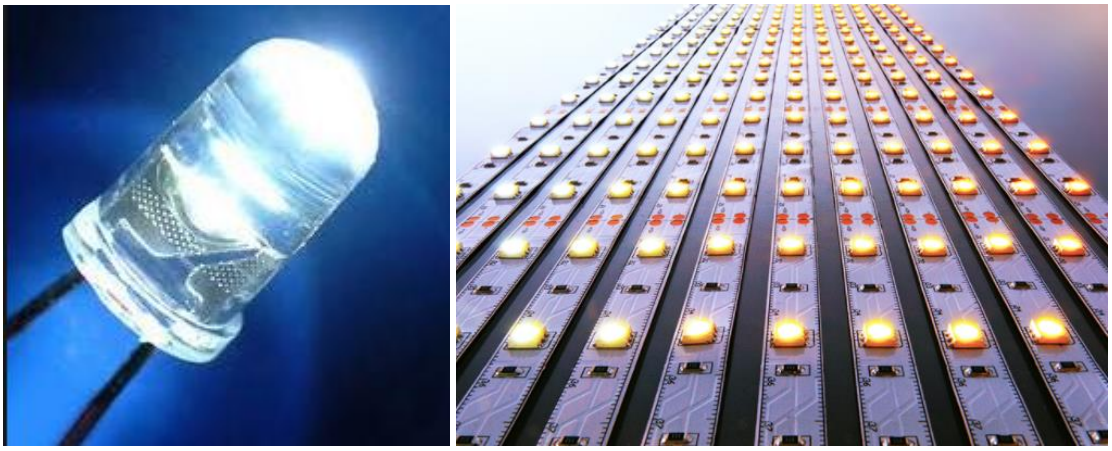
The layout of this panel of boards (boards rotated by 180°) makes necessary different cables and programming for MPU5 and MPU8

Picture 46 – Suitable and NOT suitable position on panel of boards [dimensions in mm]

4.5 Measurement of light parameters

The Flying Probe of SPEA can measure the parameters of light emitted by the LEDs mounted on the UUT as:

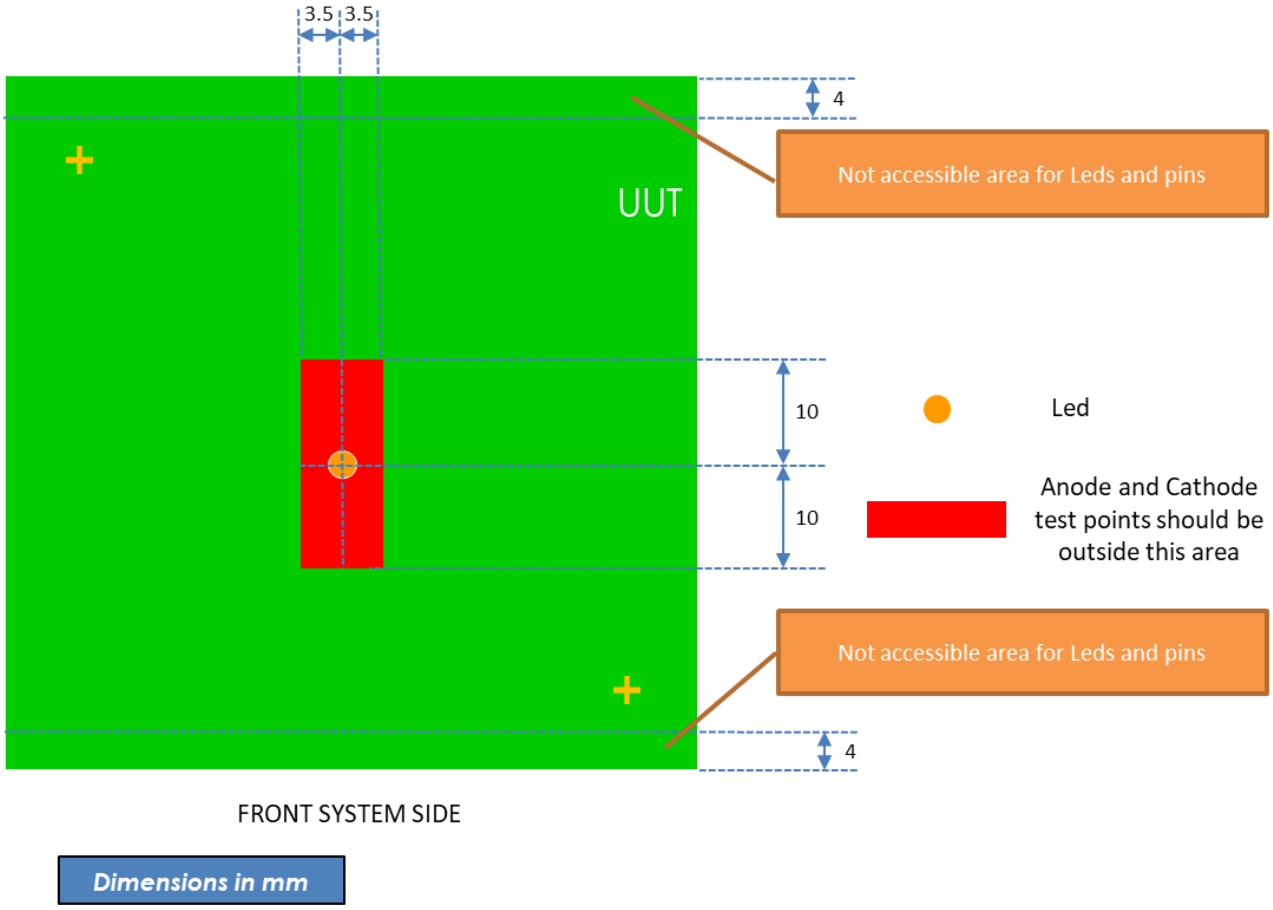
- HSL
- RGB
- Lux
- Infrared
- Binning
- Cd



Picture 47 – Examples of LEDs

4.5.1 Pins accessibility

Anode and Cathode test points of each LED should be positioned out of the area showed on the picture 48.

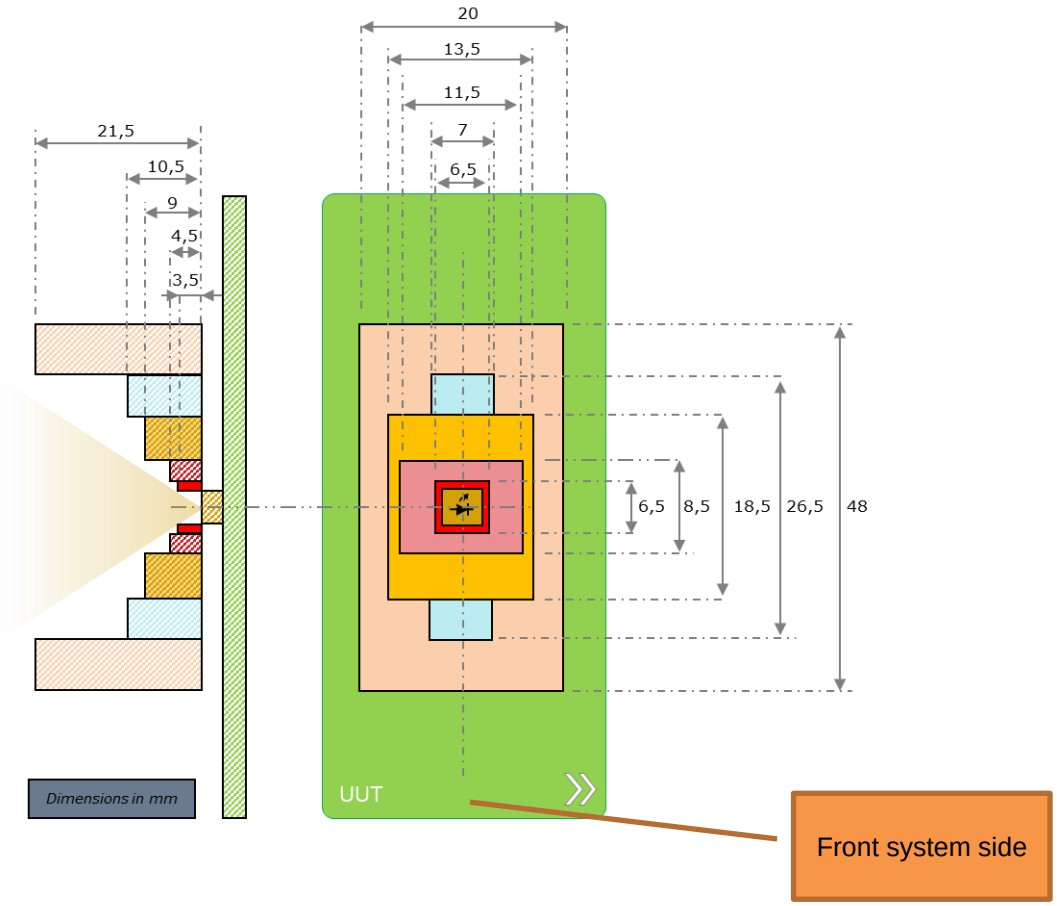


Picture 48 – Anode and Cathode test point accessibility criteria (valid for LCS55)

NOTE: this information is valid for both top and bottom sides board design

4.5.2 Height of the components around the led

Around each LED, height of components must respect the conditions described on picture 49.



Picture 49 – Accessibility surrounded Led area (valid for LCS55)

Legend:

- Area with components max height = 3,5mm
- Area with components max height = 4,5 mm
- Area with components max height = 9 mm
- Area with components max height = 10,5 mm
- Area with components max height = 21,5 mm
- Area with components max height = 55 mm

Note: all maximum heights are referred to LED's top face

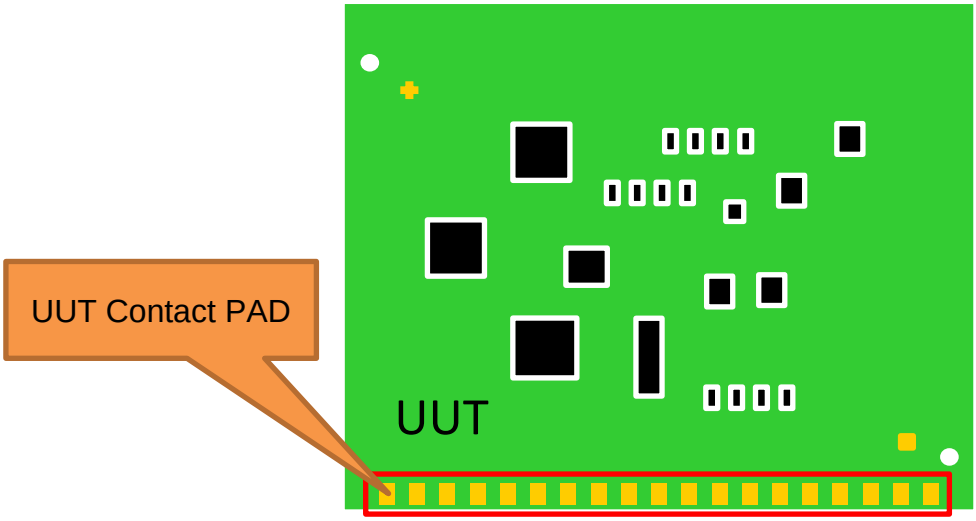
4.6 Side Device Interface (4080)

The Side Device Interface (SDI) is a contact unit which, through spring-loaded probes installed on the line clamping transports, allows signals to be applied to the UUT. Requires cards prepared with specially designed contact pads. Through the SDI you can perform tests such as:

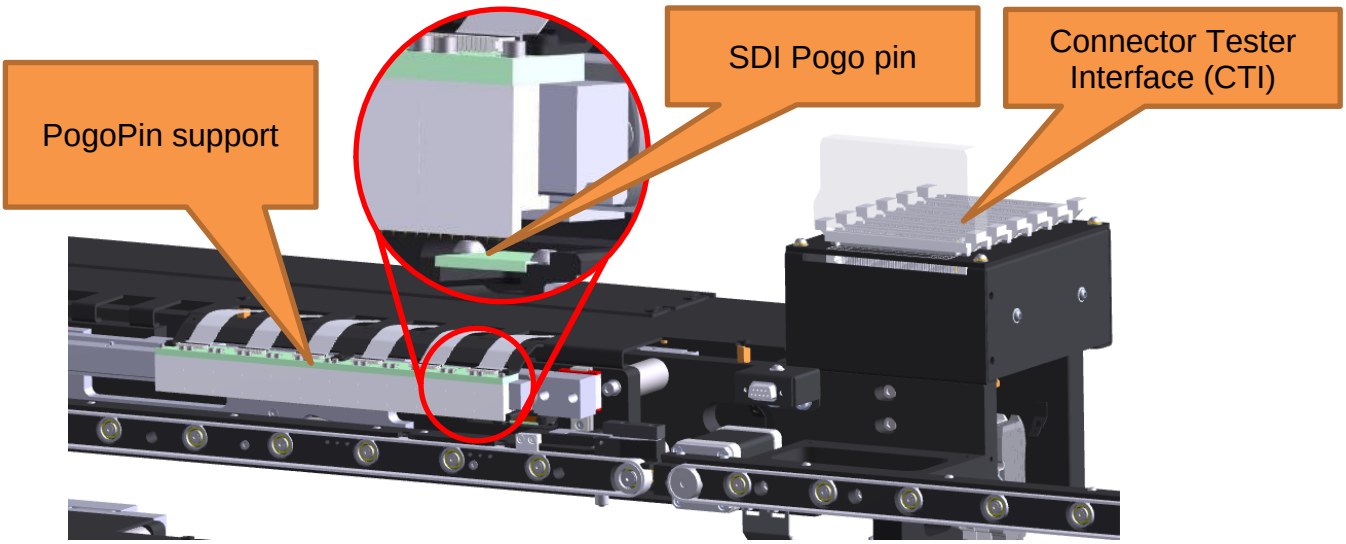
- Functional test
- Power On test
- On-Board Programming
- Boundary Scan

The information in this chapter is useful for **electronic designers** and **PCB designers** involved in the following aspects:

- Mechanical design of the pads
- Electrical connections
- Electrical connections on the board
- Electrical constraints



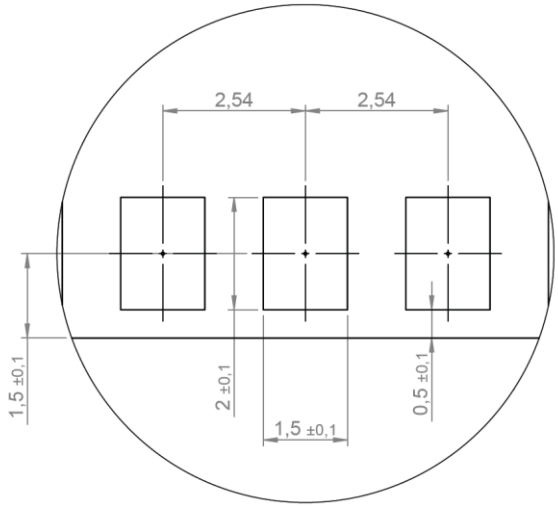
Picture 50 – Example of the SDI pod area on the UUT



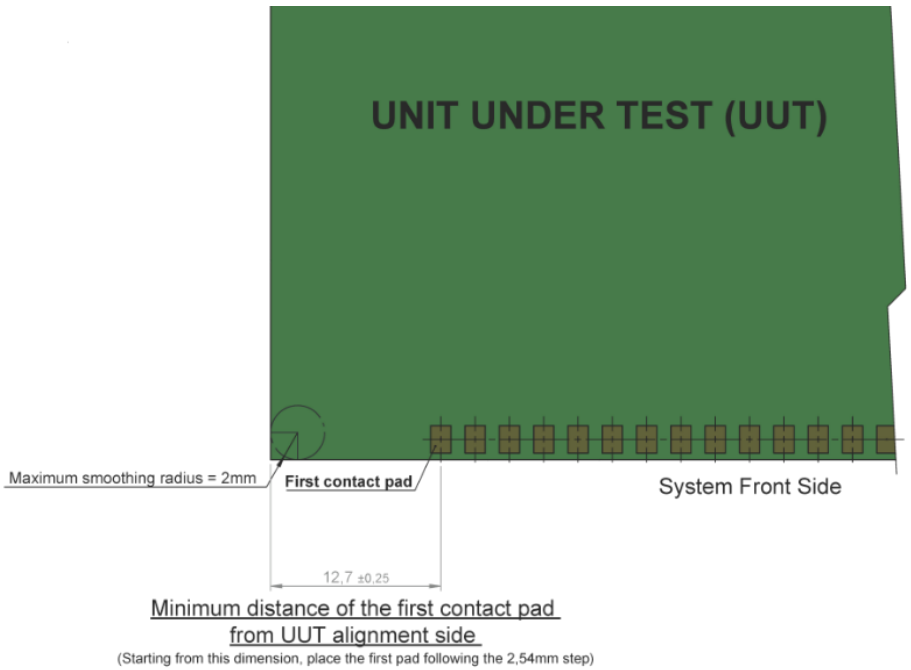
Picture 51 – SDI mechanism and detail on Pogopin

4.6.1 Mechanical design of the pads

The picture below shows the information about the shape of the pads must have to be contactable through the SDI Pogo Pin:



Picture 52 – Pad dimensions for contact via SDI [dimensions in mm]



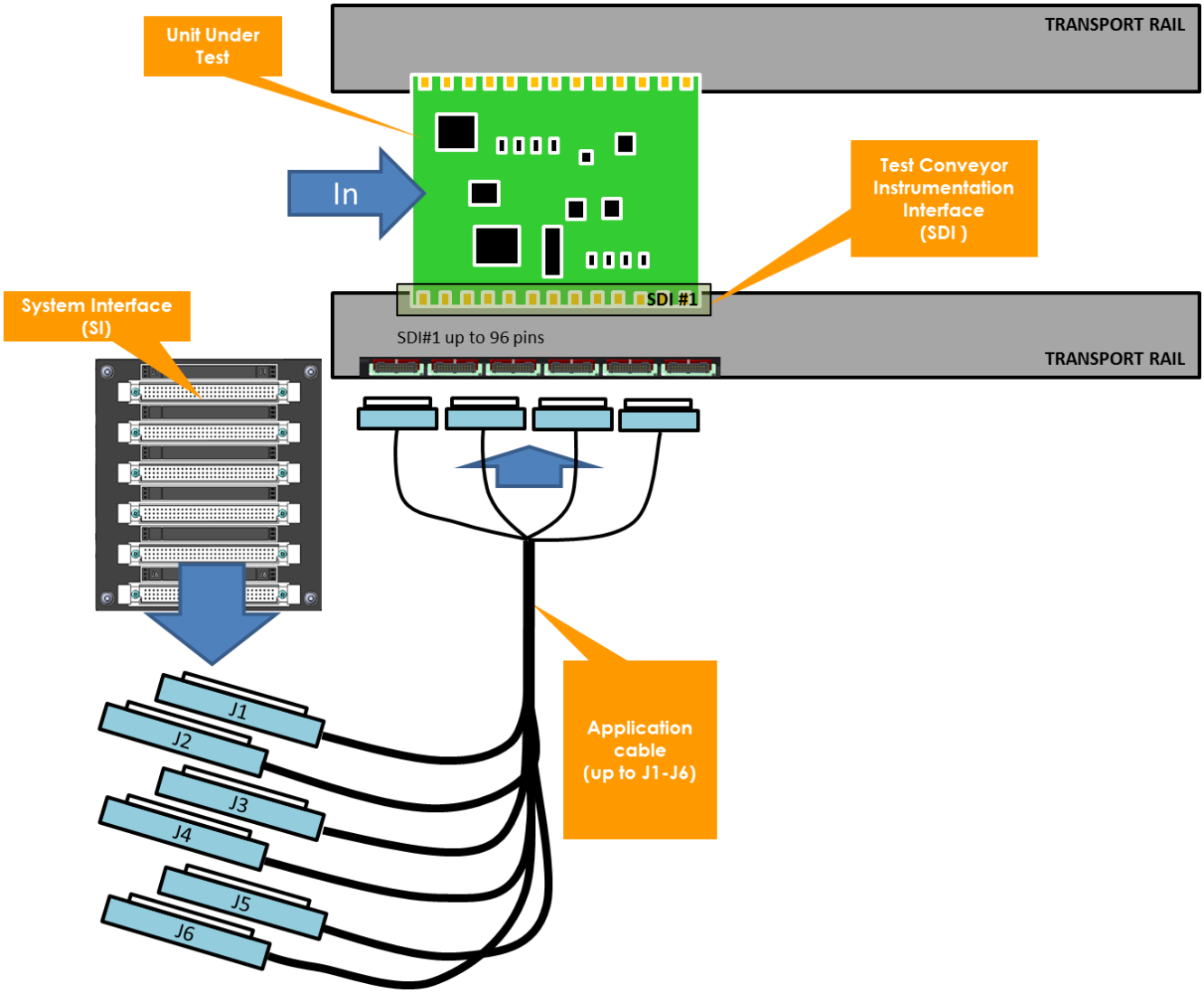
Picture 53 – Positioning of the first PAD for the contact of the Pogo Pin

Model.	Max Pins	Side
SDI120	96	Front

Table 23 – Side interface model

4.6.2 Electrical connections

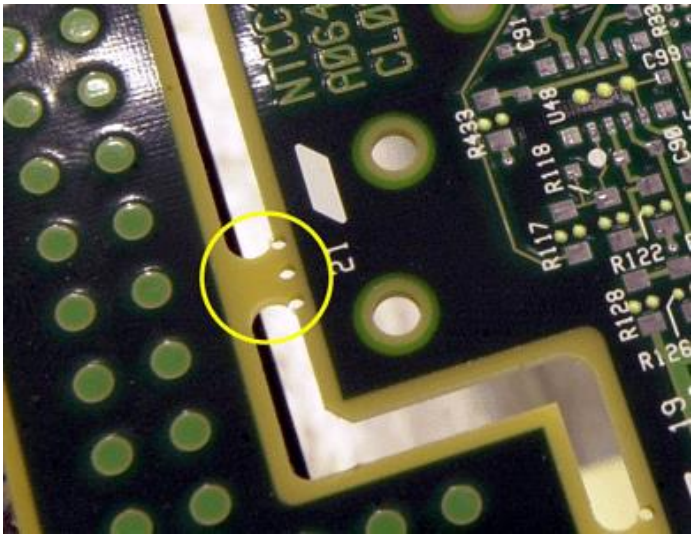
The connection of the SDI pins is completely free, in fact it is sufficient to connect the machine resource you need from the system interface to the SDI connectors.



Picture 54 – Example of connection between System Interface and SDI

4.6.3 Electrical connections on the board

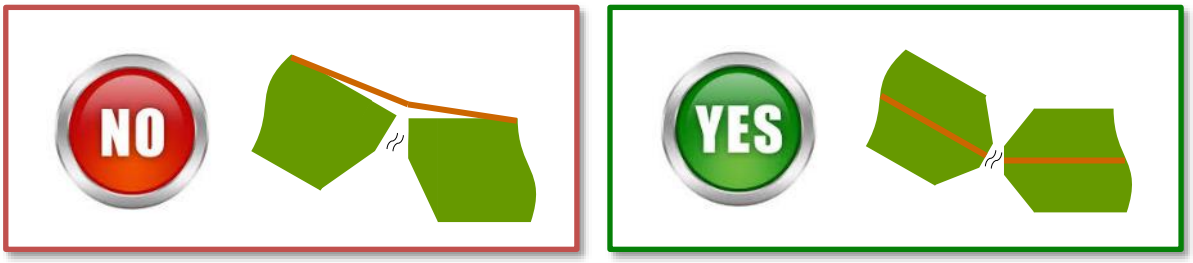
If the board is framed, for example on a board panel, it is necessary to insert tracks from the board to the PAD through supports.



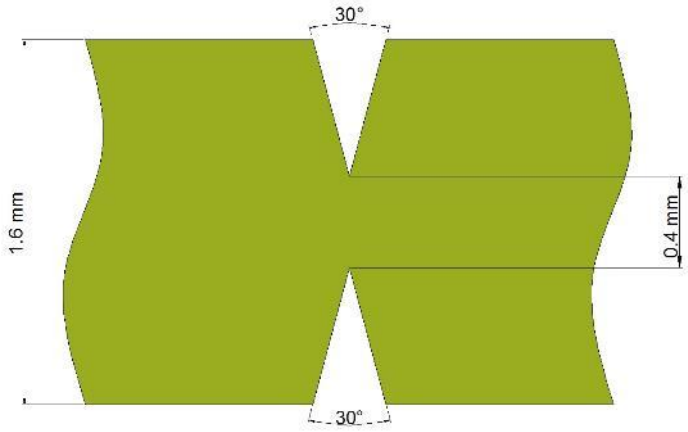
Picture 55 – Board support example

In the case of manual separation of the panel boards, the tracks must pass through the innermost layers of the PCB, in fact, passing them in the outer layers could lead to damage to the board during the division of the panel.

Each PogoPin is able to carry a maximum current of 1A, to force more current, it is necessary to create additional tracks and using more pads in parallel.



Picture 56 – Tip for separating the panel

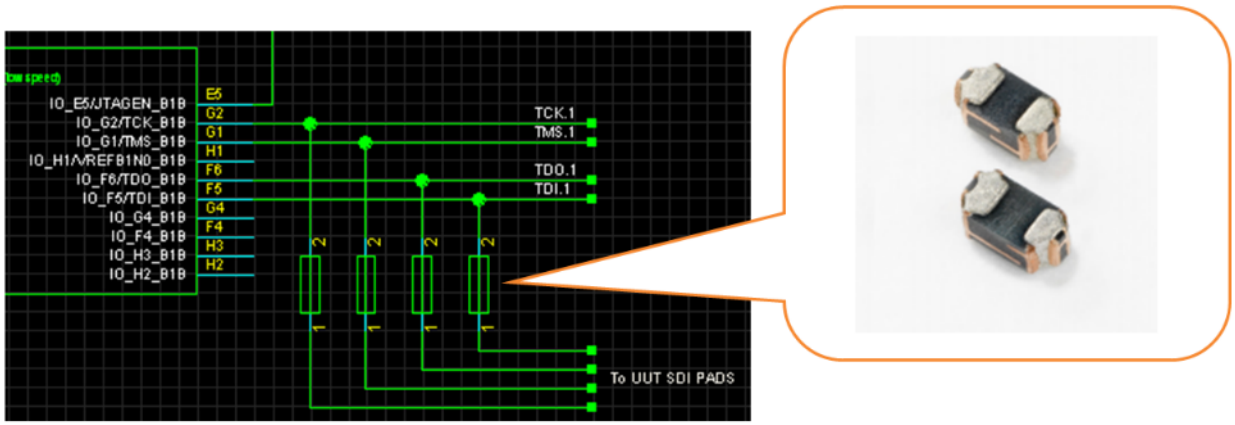


Picture 57 – V-Groove Scoring

4.6.4 Electrical constraints

If the Pads are on the panel frame, you need to divide the tracks that lead to the PADs from the rest of the circuit, to avoid creating parasitic stubs.

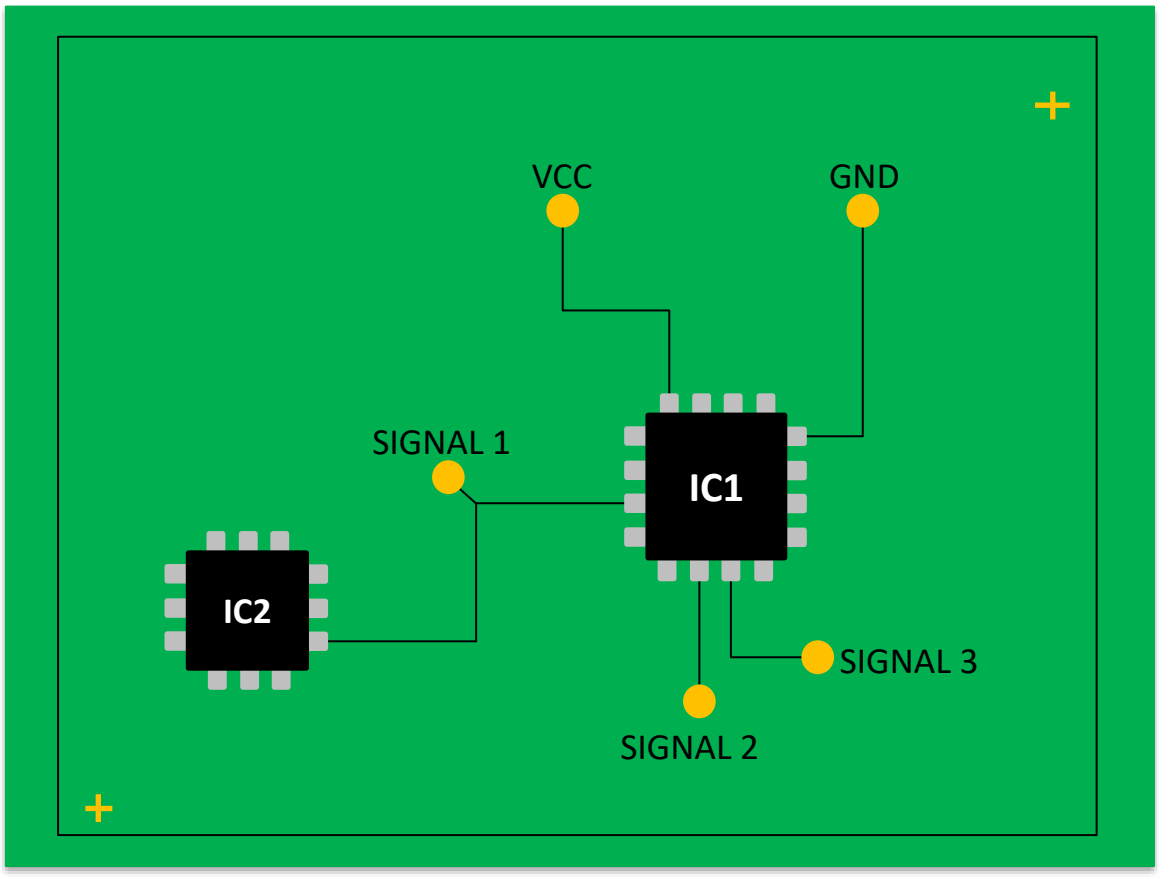
An example of division of the tracks is to place fuses near the intersection of the net, and at the end of the test burn them.



Picture 58 – Example of circuit and fuses for the division of the net

4.7 Programmable components

The Flying Probe allows the programming of the programmable components during the execution of the test program.
Depending on the required programming signals and the necessary power supplies, programming can be carried out in different ways indicated in this chapter.



Picture 59 – Example of programmable component and relative accessibility

4.7.1 Pre-requisites for accessibility and constraints

To program a component it is suggested to take care of the following aspects:

- Total accessibility of all the points involved in the programming.
- Total accessibility of power nets from multiple points.
- Total accessibility of other signals needed for programming (constraints, pull-ups, pull-downs, ...)
- Total accessibility of all the signals necessary for disabling the component to be programmed or other programmable components (reset, ...)
- As far as possible, do not connect directly to VCC or GND the signals involved in the programming (restraints, reset, signals to force specific voltages ...).
- Provide, if possible, a status of the board that confirms the successful programming (LED, H / L signal, current absorption different from the unscheduled card, ...).
- Provide accessibility and the possibility to disable any oscillators.

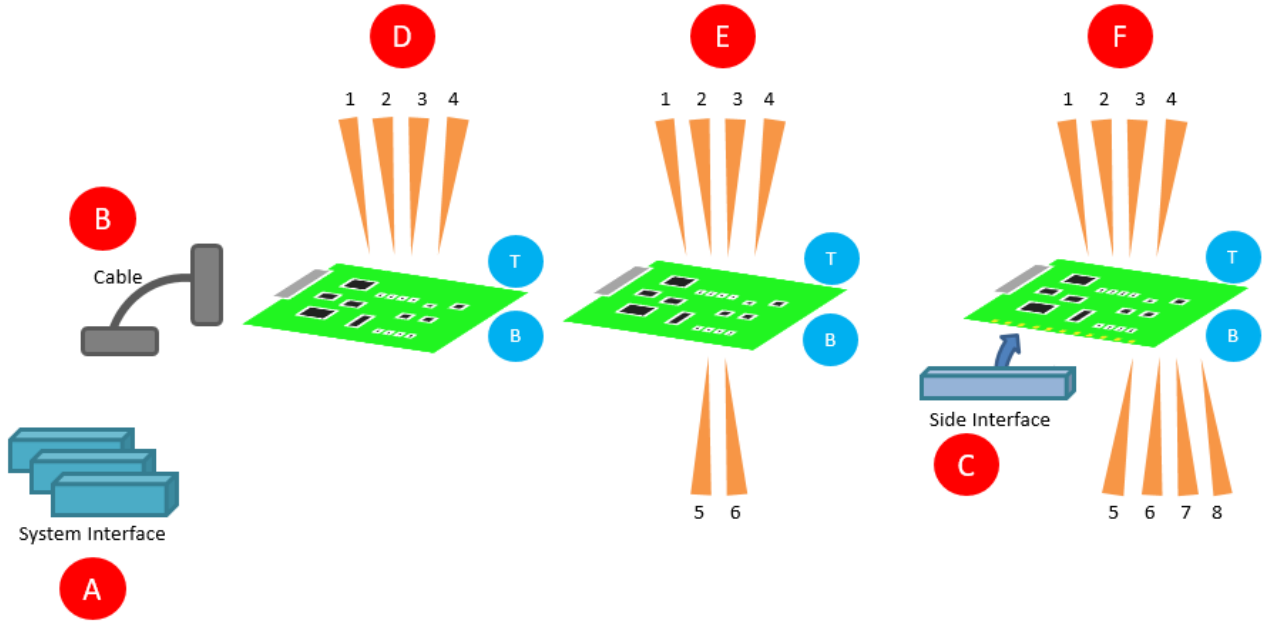
4.7.2 OTP components

In case of use of OTP components, it is recommended to install, for debugging operations, other programmable versions of the component (even if they have a different type of case) in which it is possible to perform more than one single programming.

4.7.3 Programming of several components connected to each other

The simultaneous programming of different devices is not applicable if the components in question are short-circuited.
Decoupling resistors on the programming bus must be provided between programmable components.

4.7.4 Accessibility combinations



Picture 60 – Accessibility combinations

Component programming signals	A System Int.	B Cable	D 4-Axis System	E 6-Axis System	F 8-Axis System	Signals Programming Access	Signals Power Access
Up to 2-Wires	-	-	X	-	-	T	T
Up to 2-Wires	-	-	-	X	-	T	T or B
Up to 2-Wires	-	-	-	-	X	T or B or C	T or B or C
Up to 4-Wires (1)	X	X	X	-	-	T	Connector or B
Up to 4-Wires	-	-	-	X	-	T	B
Up to 4-Wires	-	-	-	-	X	T or B or C	T or B or C
Up to 6-Wires (1)	X	X	X	-	-	Connector	Connector
Up to 6-Wires (1)	X	X	-	X	-	T + B	Connector
Up to 6-Wires	-	-	-	-	X	T + B or C	T + B or C
Up to 8-Wires (1)	X	X	X	-	-	Connector	Connector
Up to 8-Wires (1)	X	X	-	X	-	Connector	Connector
Up to 8-Wires	-	-	-	-	X	T + B or C	T + B or C

(1) Manual loading system

Table 24 – Recommended combinations in the accessibility of programming and power signals according to the system model